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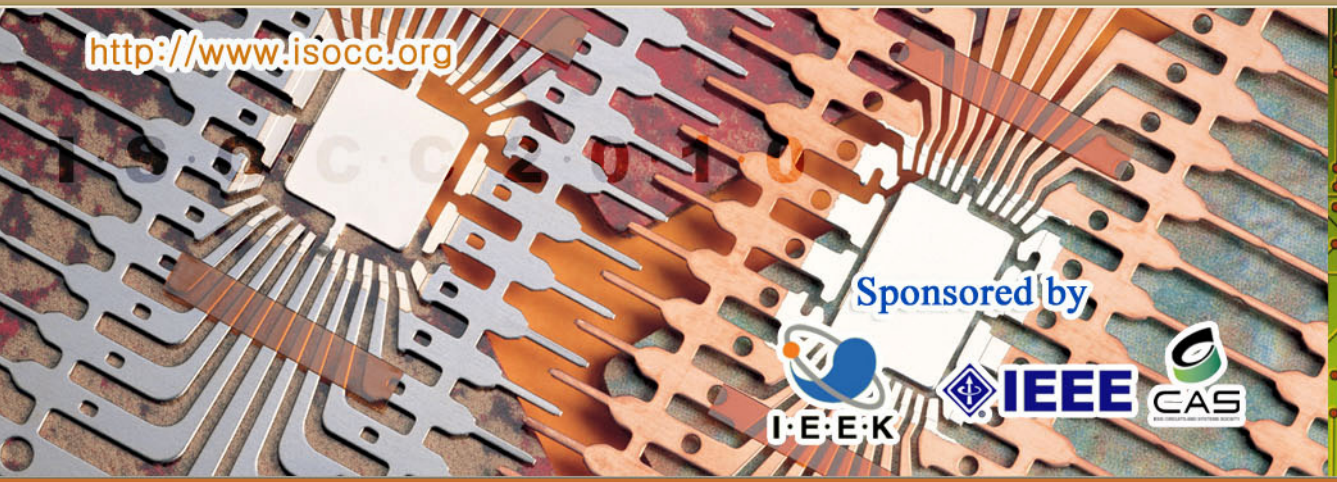

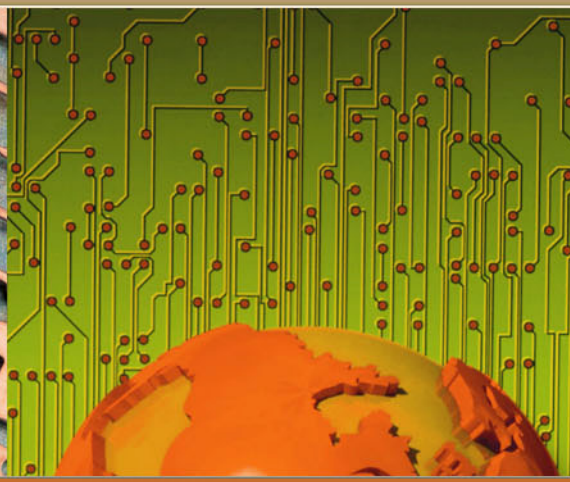

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4-Channel 3.2/6.4-Gbps Dual-rate Transmitter

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I. INTRODUCTION

As the speed of A/V streaming increases, the transmission-speed requirement of many serial links is continuously increasing. With this, providing flexibility between previous and new versions of serial links for many commercial standards becomes important. This paper demonstrates 4-channel 3.2/ 6.4 Gbps transmitter, in which different amounts of pre-emphasis as well as output swings can be selected. The prototype chip was fabricated using 0.13μm CMOS process.

II. DESCRIPTION

The block diagram of the transmitter is shown in Fig. 1. Each of 4 transmitters consists of parallel pattern generator, 16:2 serializer, and pre-emphasis circuit. All 4 transmitters share one PLL as a clock generator, which provides clocks having frequencies of f/16, f/8, f/4, and f/2. The desired clock frequency can be selected by an external control signal. The parallel pattern generator offers 16-bit random data having f/16 data rate. 16:2 serializer converts 16-bit data into 2-bit data using clocks of f/16, f/8, and f/4 frequencies. Pre-emphasis circuit serializes 2-bit data to 1-bit data using f/2 frequency clock, and controls the amount of output swing and pre-emphasis.

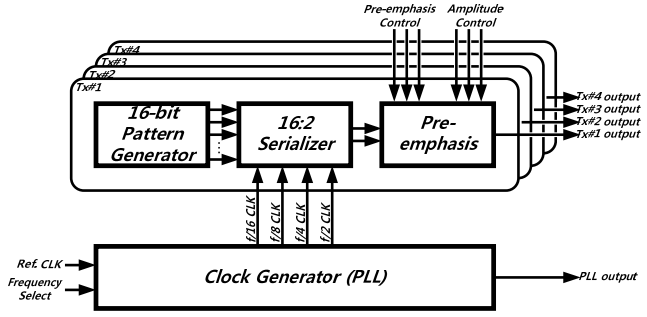

Fig. 1. Block diagram of transmitter

III. CHIP IMPLEMENTAION AND RESULTS

The prototype chip was fabricated using Samsung 0.13μm CMOS process. The area of each transmitter is 300×300μm^2 and the area of PLL is 300×400μm^2. Fabricated chip is assembled on board with COB (chip on board) packaging and consumes 600mW from 1.2V supply. PLL operates at 3.2GHz with 7.573ps$_{rms}$of jitter. Fig. 2 shows measurement results of pre-emphasis and output swing control.

Table 1. Performance of fabricated chip

Process	Samsung 0.13 μm CMOS
Data Rate	3.2 / 6.4 Gbps
Supply Voltage	1.2 V
Power Consumption	600mW (4ch. Tx + PLL)
Pre-emphasis	1x / 1.5x / 2x / 3x
Output Swing	200 / 300 / 400 / 600 mV$_{diff,p2p}$
PLL jitter	7.573 ps$_{rms}$
Area	300 × 400 μm^2 (Tx 1ch.) 300 × 300 μm^2 (PLL) 2500 × 900 μm^2 (including pads)
Transmitter Jitter	31.9 ps$_{p2p}$ (3.2Gb/s) 44.3 ps$_{p2p}$ (6.4Gb/s)

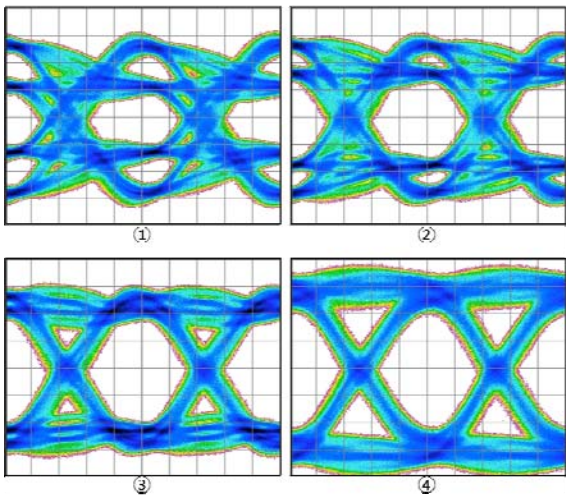

Fig. 2. Measured transmitter output; (1) pre-emphasis 3x, 200mV$_{diff,p2p}$ (2) pre-emphasis 2x, 300mV$_{diff,p2p}$ (3) pre-emphasis 1.5x, 400mV$_{diff,p2p}$ (4) without pre-emphasis 600mV$_{diff,p2p}$

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