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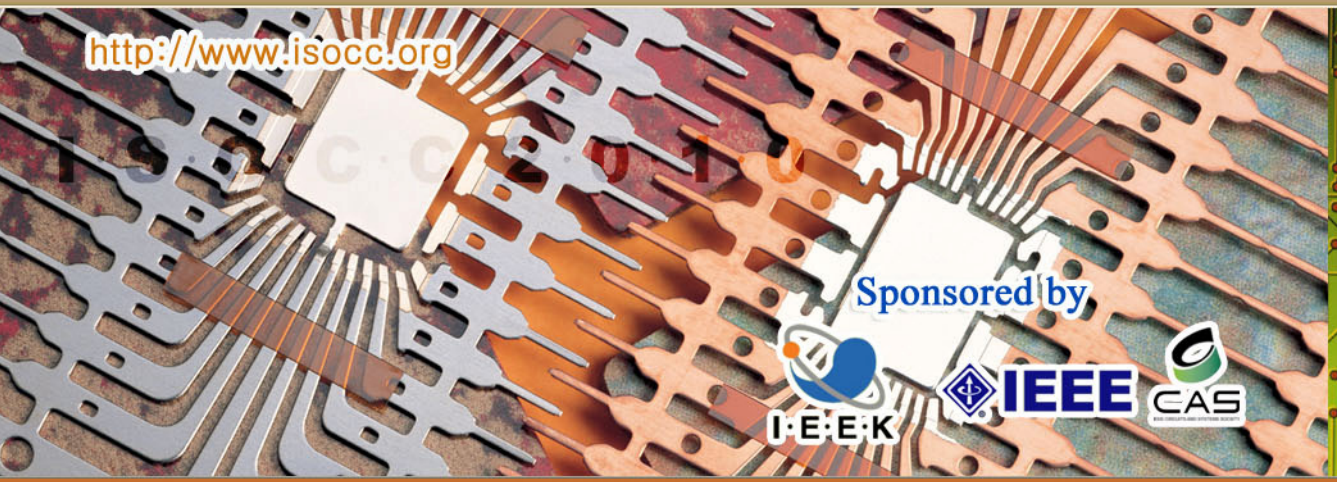

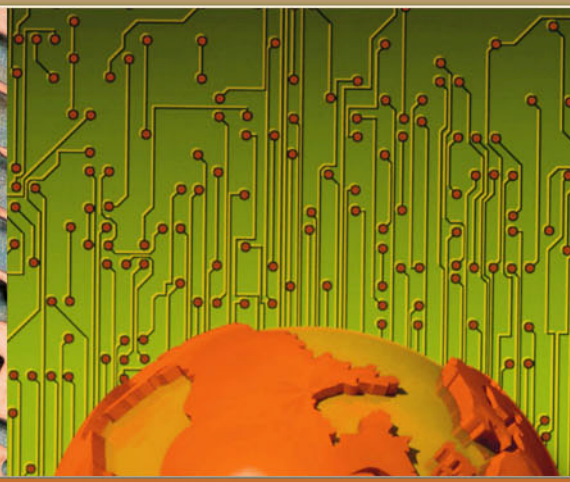

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Technical Support : Kyung Min D&P Co. Phone : 82-2-2269-1849 FAX : 82-2-2269-1846 E-mail : kim1849@korea.com

1.62 and 2.7 Gb/s Dual-rate Adaptive Equalizer

Jinsoo Rhim, Chang-kyung Seong, Wangsoo Kim, and Woo-young Choi
Dept. of Electrical and Electronic Engineering
Yonsei University, Seoul, Korea
peter@tera.yonsei.ac.kr

I. INTRODUCTION

Since the data rate of communication systems is limited by the channel bandwidth, various techniques have been introduced. Equalization is the most widely used solution for serial link systems in high speed communication. In this paper, an adaptive equalizer is successfully demonstrated through 15m DisplayPort cable at 1.62 Gb/s and 2.7 Gb/s.

II. DESCRIPTION

Figure. 1 shows the overall structure of our equalizer. It consists of two parts: equalizer filter which compensates the degraded high frequency components and the adaptation block which controls the amount of equalization.

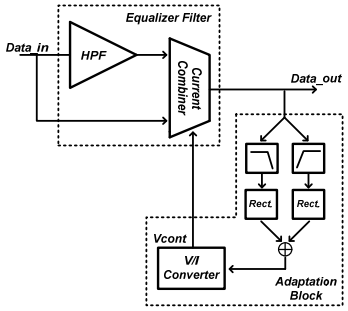

Fig. 1. Block diagram of the adaptive equalizer

A high-pass filter with current combiner boosts up the degraded high frequency components due to the limited channel bandwidth. The current combiner is a current-mode logic (CML) buffer with two different inputs as shown in fig. 2.

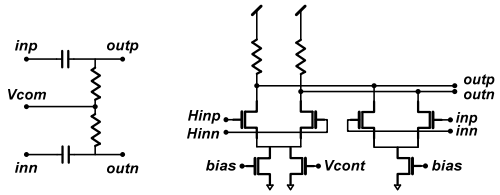

Fig. 2. Schematic of (a) High-pass filter (b) Current combiner

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The adaptation block compares high and low frequency components of the signal after the filter and controls the current combiner for proper amount of compensation.

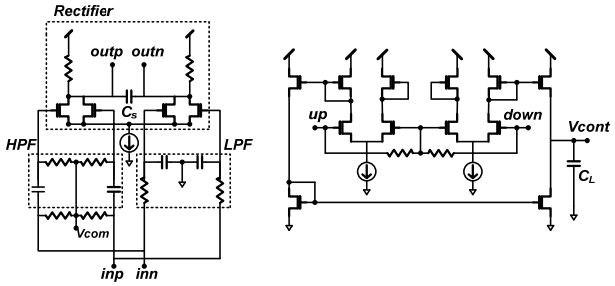

Fig. 4. Schematic of (a) Rectifier (b) V/I converter

III. CHIP IMPLEMENTAION AND RESULTS

The chip is fabricated with 0.13μm CMOS technology and occupies the area of 115 μm x 115 μm and consumes 11mW of power. Figure 4 shows the signal before and after equalizer for 1.62 Gb/s (left) and 2.7 Gb/s (right).

Table 1. Performance summary of fabricated chip

Technology	Chartered 0.13μm CMOS Process
Operation Speed	1.62 Gb/s, 2.7 Gb/s
Power consumption	11mW (excluding output buffer)
Chip Area	115 x 115 μm^2

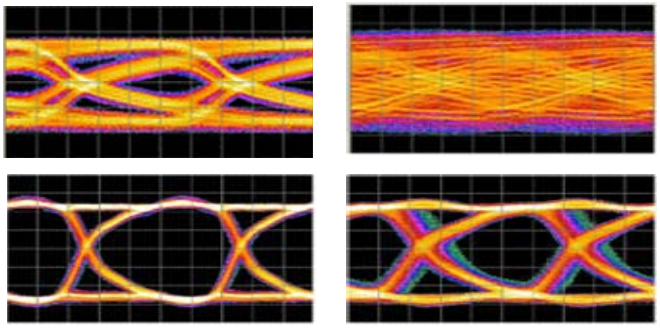

Fig. 4. Eye diagram before and after equalizer