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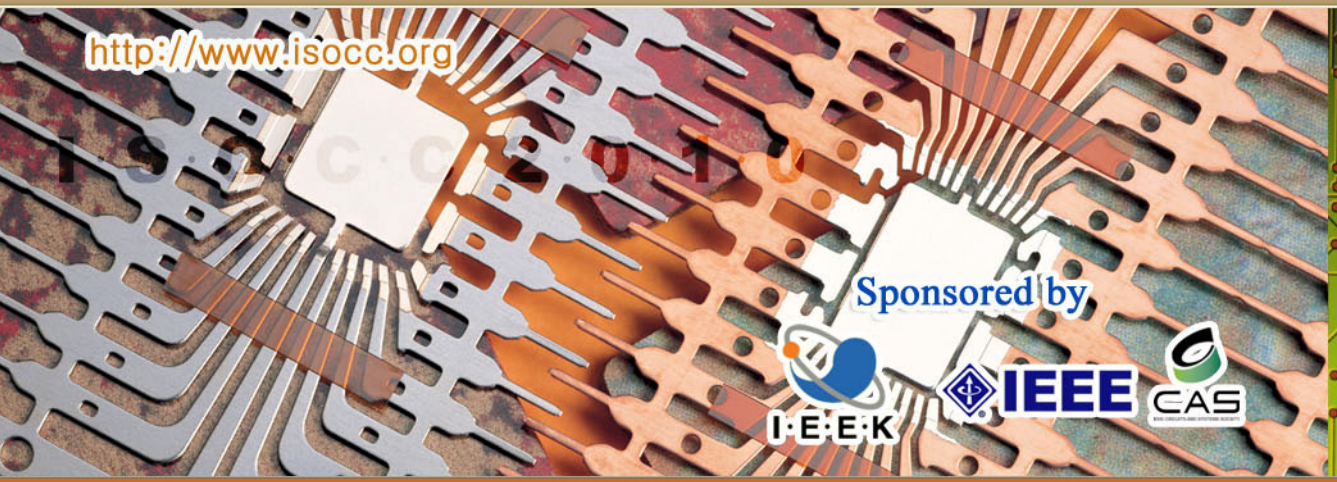

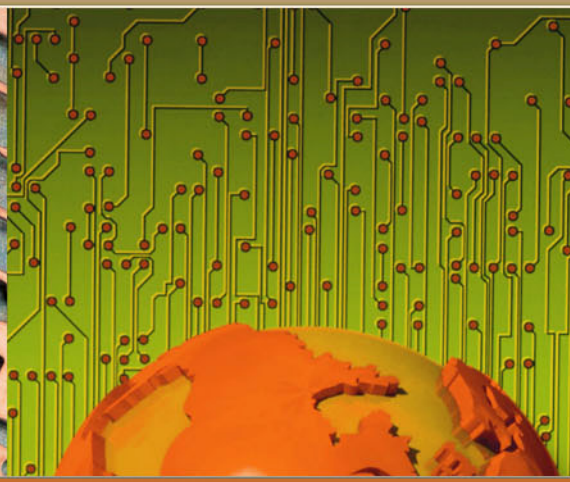

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6.25-Gb/s Optical Receiver Analog Front-End in a 0.13-μm CMOS Technology

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I. INTRODUCTION

As data transmission capacity increases in many electronic interconnect applications, existing electrical interconnects face severe problems due to large channel loss, noise and power consumption. In order to solve these problems, there are active research efforts to realize high-speed optical receivers for optical interconnect applications. In this paper, we demonstrate the optical receiver front-end in a 0.13-μm CMOS technology.

II. DESCRIPTION

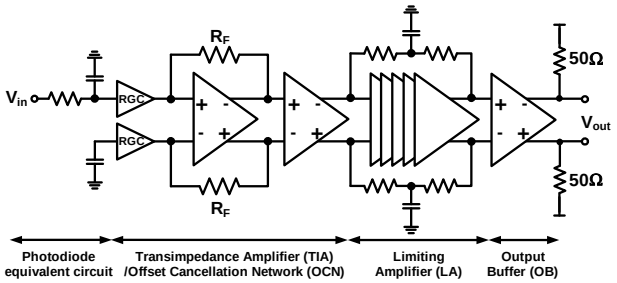

Fig. 1. Simplified architecture of the CMOS optical receiver analog front-end.

Fig. 1 shows the simplified block diagram of the fabricated CMOS optical receiver front-end. The CMOS optical receiver is composed of photodiode equivalent circuit, transimpedance amplifier (TIA), offset cancellation network (OCN), limiting amplifier (LA), and output buffer.

In photodiode equivalent circuit [1], resistor and capacitor play the role of the voltage-current converter and parasitic junction capacitance of photodiode, respectively. The TIA is composed of regulated cascode (RGC) [1], feedback amplifier having two-stage differential amplifier. The RGC can effectively isolate input parasitic capacitance. The OCN having two low-pass filters and f_T-doubler converts the pseudo-differential signal into a fully-differential signal. The limiting amplifier consists of five-stage amplifiers and each amplifier is composed of a two-stage differential amplifier with active feedback. With the active feedback, core amplifier bandwidth can be increased beyond f_T [2]. The output buffer is used for driving 50-Ω loads.

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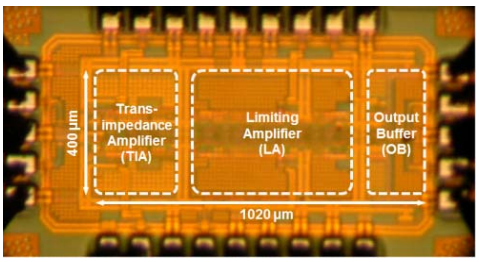

Fig. 2. Microphotograph of the fabricated CMOS optical receiver analog front-end.

Fig. 2 shows the microphotograph of the fabricated CMOS optical receiver analog front-end. The core chip size is about 1020 μm x 400 μm and total power consumption excluding output buffer is about 68 mW with the 1.2 V supply voltage.

III. CHIP IMPLEMENTAION AND RESULTS

With fabricated CMOS optical receiver, data transmission measurement was conducted. The pseudorandom bit sequence (PRBS) of 2^{31}-1 was generated by a pulse pattern generator (PPG) and this voltage signal was converted into current signal having about 100-μA_{pp} swing. Fig. 3 shows the measured eye diagrams when 4.25-Gb/s and 6.25-Gb/s data were transmitted.

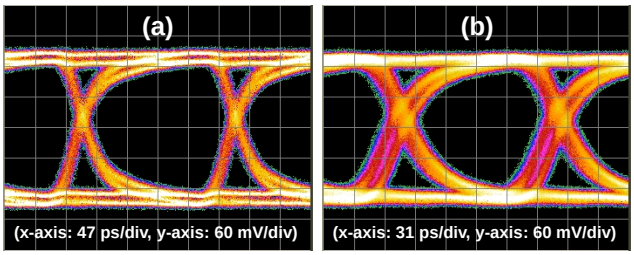

Fig. 3. Measured eye-diagram of (a) 4.25-Gb/s (b) 6.25-Gb/s data when input current swing is about 100 μA_{pp}.

REFERENCE

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