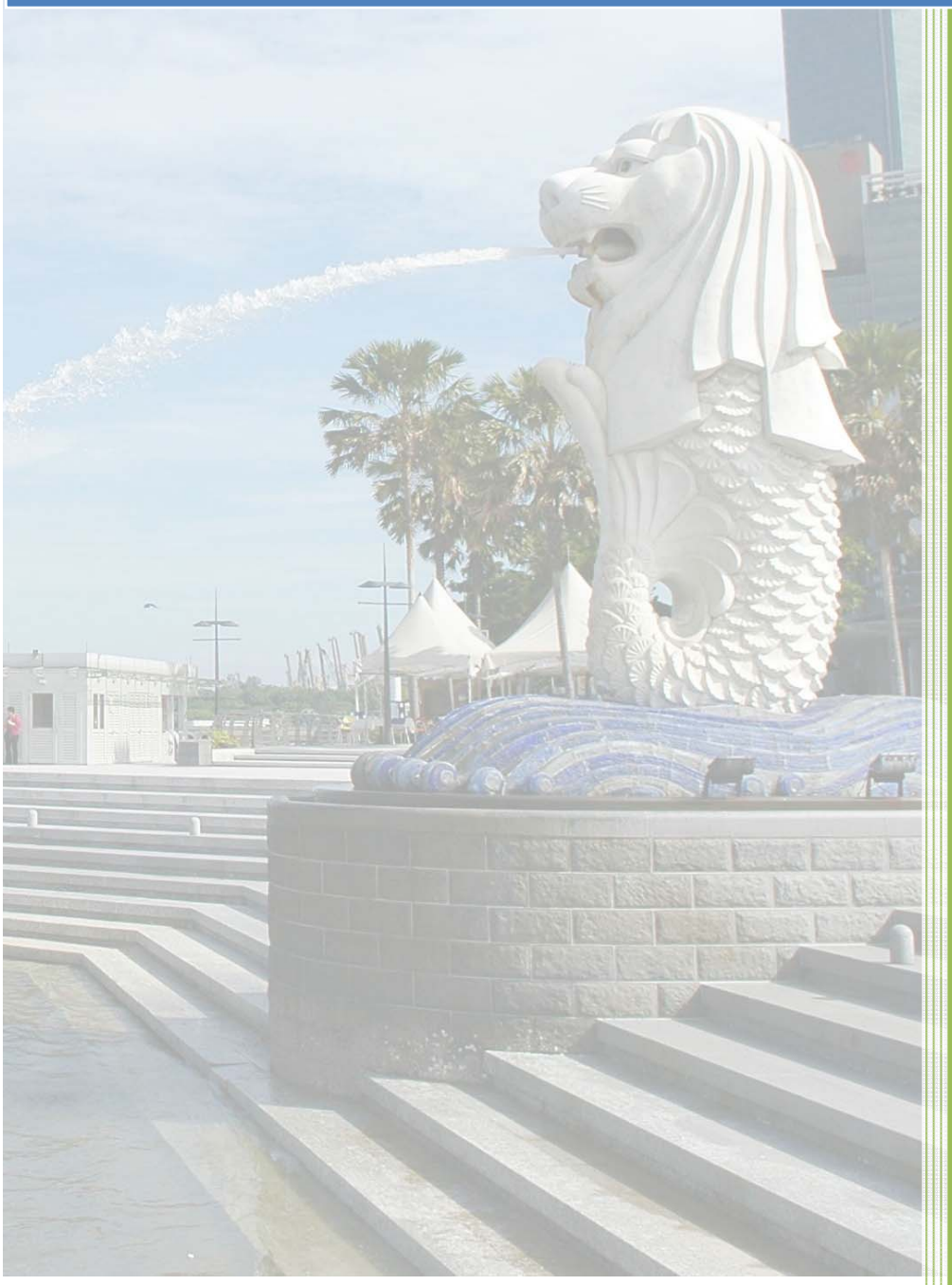
NANYANG TECHNOLOGICAL UNIVERSITY

IEEE SINGAPORE SECTION

ISIC-2009



12th International Symposium on Integrated Circuits

14-16 December 2009

Suntec Singapore International Convention & Exhibition Centre

Proceedings

Front Matter

Supported by:

SINGAPORE EXHIBITION & CONVENTION BUREAU

SSCS

M.I.D.A.S. Singapore's Semiconductor Community

Held in:

UNIQUELY Singapore
www.visitsingapore.com

Wednesday, 16 Dec 2009

C6 **Special Session 7: High-speed and Low-complexity Implementation of Communication Systems**
Time: Wednesday, 16 Dec 2009, 15:30 – 17:20
Room: 310
Chair: Younglok Kim

15:30
C6-1 **Performance Comparison of Various Post Processing Algorithms**
Changtaek Shin, Jinyoung Lee, Jungjun Park, Younglok Kim, *Korea* (*Invited Paper*)

15:48
C6-2 **High-speed Low-complexity Folded Degree-computationless Modified Euclidean Algorithm Architecture for RS Decoders**
Hyo-Jin Ahn, Chang-Seok Choi, Hanho Lee, *Korea*

16:06
C6-3 **Linear Analysis and Speed Maximization of Feed Forward Ring Oscillators**
Young-Seok Park, Pyung-Su Han, Woo-Young Choi, *Korea*

16:24
C6-4 **1.25 Gb/s Burst-mode CMOS PON Laser Diode Driver with Automatic Power Controller**
Young Joo Lee, Eun Chul Kang, Jinwook Burm, *Korea*

16:42
C6-5 **Design of Remote Management System with ZigBee**
Jeongsoo Park, Taewan Kim, Yunmo Chung, *Korea*

17:00
C6-6 **Design of Wide-Bandwidth Sigma-Delta Modulator for Wireless Transceivers**
Jungsu Choi, Kichang Jang, Junsang Lee, Wooju Jeong, Jungeui Park, Jayang Yoon, Seok Lee, Joongho Choi, *Korea*

Linear Analysis and Speed Maximization of Feed Forward Ring Oscillators

Young-Seok Park[(1)], Pyung-Su Han[(2)], Woo-Young Choi[(1)]

Department of Electrical and Electronic Engineering,
Yonsei University[(1)]
Seoul, Korea
circuit@tera.yonsei.ac.kr

Department of System IC Business,
LG electronics[(2)]
Seoul, Korea
pshan@lge.com

***Abstract*—A linear model for feed forward ring oscillators (FROs) is developed and the oscillator characteristics are analyzed using the model. The model allows the prediction of multiple oscillation modes as well as the oscillation frequency of each mode. Prediction based on the model agrees well with SPICE simulation results. Using the model, a five-stage FRO is optimized for its highest oscillation frequency. Post-layout simulation shows that 12-GHz oscillation frequency is achievable with a typical 0.18-µm CMOS technology.**

***Index Terms*—feedforward ring oscillator, ring oscillator, oscillator analysis, oscillation frequency maximization**

I. INTRODUCTION

Ring oscillators are very useful. Except for RF systems where extremely low phase noises are essential, ring oscillators having small sizes, power efficiency, tunability, and ease of integration with digital logic circuits are the best choice for clock generators. In addition, a ring oscillator can generate multiphase clock signals, which are very useful for many applications such as clock recovery circuits and digital DLLs.

The oscillation frequency, f_{OSC}, for a ring oscillator is can be given as

$$f_{OSC} = 1/(2Nt_d), \quad (1)$$

where N is the number of stages, and t_d is propagation delay of the unit stage. Designers have to choose a unit stage structure having small t_d in order to achieve high oscillation frequency. Source-coupled differential amplifiers are usually used, but they typically have large power consumption and small output swing.

To overcome these limitations, several types of ring oscillator structures have been investigated [1]-[8]. Although they are called by different names, such as dual delay path oscillators [2], sub-feedback oscillator [3], feed forward oscillators [5], all of them have feed forward paths in common. Some of them [7] are very fast even compared with LC oscillators. Some of them utilize even numbered inverter rings [1], [3]-[5], which is impossible for conventional single path ring oscillators.

Despite their usefulness, feed forward ring oscillators have not been analyzed systematically and designers have to rely on trial-and-error approaches. In this paper, a new analytical model of feed forward ring oscillator is presented, which can be easily used for design optimization.

II. ANALYSIS OF FEED FORWARD RING OSCILLATORS

A. Frequency Response

In a ring oscillator the oscillation condition is achieved if signals in the oscillator experience phase shifts corresponding to multiples of 2π and amplitude gain greater than unity during a circular trip around the loop. Fig. 1 depicts the schematic diagram of a five-stage feed forward ring oscillator given in [6]. We can define the FRO unit stage as the simplest repeating circuit fragment as shown in Fig. 2. In this figure, α represents scaling factor for the feed forward path inverting amplifier, which is α times larger than the direct path inverting amplifier.

When oscillating is achieved, the oscillator output signals, i.e. ck0-ck4, have constant-and-equal phase relationships. In other words, any two adjacent nodes have the same phase angle difference θ. There are four possible θ's as shown in fig. 3. Among those four angles, only $\theta_2 = 4\pi/5$ is concerned for the conventional single path five-stage ring oscillator because it is the only one that can satisfy the oscillator's phase condition.

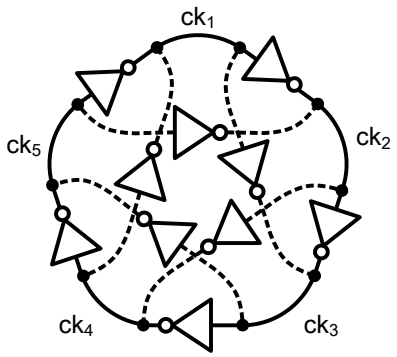


Figure 1. A schematic diagram of five-stage FRO.

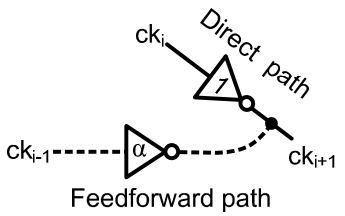


Figure 2. Unit stage of the five-stage FRO.

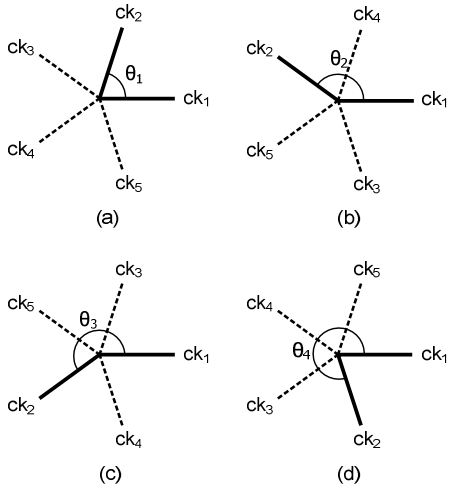


Figure 3. Four phase values of five-stage FRO for possible oscillation; (a) $\theta_1=2\pi/5$ (b) $\theta_2=4\pi/5$ (c) $\theta_3=6\pi/5$ (d) $\theta_5=8\pi/5$

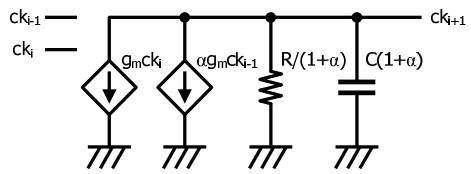


Figure 4. A small-signal equivalent circuit of the uit stage

The small signal equivalent circuit of the unit stage made up of a simple inverting amplifier is shown in Fig. 4. The resistor in Fig.4 represents two parallel resistors, R from the direct path and R/α from the feed forward path. The two parallel capacitors, C and αC, are also shown as a single capacitor, C(1+α). The output signal ck_{i+1} can be expressed as function of two input signals, $ck_{i-1}$and ck_i, as

$$ck_{i+1}=\frac{-g_m R}{(1+\alpha)(1+j2\pi fRC)}(ck_i+\alpha ck_{i-1}) \tag{2}$$

For an oscillator in stable oscillation, signals at any two nodes have constant phase relationship and (2) can be rewritten with ck_{i-1} substituted by $ck_i\exp(-j\theta_k)$. Then ck_{i+1} can be expressed as a function of ck_i as

$$ck_{i+1}=G(\alpha)ck_i,\ where\ G(\alpha)=\frac{-g_m R[1+\alpha\exp(-j\theta_k)]}{(1+\alpha)(1+j2\pi fRC)}. \tag{3}$$

The phase response of G(α) can be expressed as

$$\angle G(\alpha)=\pi+\beta-\gamma, \tag{4}$$

where β and γ represent the frequency-independent and frequency-dependent portion of the phase response, respectably, as given below:

$$\beta=\begin{cases}\tan^{-1}(Y/X), \text{ if } X>0\\ \tan^{-1}(Y/X)+\pi, \text{ if } X<0\end{cases}$$

, where $X=1+\alpha\cos\theta_k$, $Y=-\alpha\sin\theta_k$. (5)

$$\gamma=\tan^{-1}(2\pi f_{OSC}RC). \tag{6}$$

In Fig 5, the phase relationship between ck_{i-1}, ck_i and ck_{i+1} are depicted as vectors on a complex plane. In the figure, phase angle β is introduced by the feed-forwarded signal ck_{i-1}, which is lagging ck_i by θ_k. Since θ_k is constant in a specific oscillation mode, β is independent of the oscillation frequency and is determined solely by the feedforward strength α. To achieve oscillation in that mode, ck_i should be also lagging ck_{i+1} by θ_k or,

$$\pi+\beta-\gamma=\theta_k. \tag{7}$$

Using (6) and (7) we have

$$0\le\gamma=\pi+\beta-\theta_k<\pi/2. \tag{8}$$

The magnitude response of G(α) can be determined from (3), (5), (6) and (7).

$$|G(\alpha)|=\frac{g_m R}{(1+\alpha)}\sqrt{\frac{X^2+Y^2}{1+\tan^2(\theta_k-\beta)}}$$

$$=\frac{-g_m R}{(1+\alpha)}\sqrt{X^2+Y^2}\,(X\cos\theta_k+Y\sin\theta_k)=\frac{-g_m R}{(1+\alpha)}(\cos\theta_k+\alpha\cos 2\theta_k). \tag{9}$$

Whether a given set of k and α can result in an oscillating FRO or not can be determined by checking first if γ given in (8) satisfies $0\le\gamma<\pi/2$ and, then $|G(\alpha)|$ in (9) is larger than one. The corresponding oscillation frequency f_{OSC} can be calculated using (5), (6) and (7) as following:

$$f_{OSC}=\frac{\tan\gamma}{2\pi RC}=\frac{\tan(\beta-\theta_k)}{2\pi RC}=\frac{1}{2\pi RC}\left(\frac{(Y/X)-\tan\theta_k}{1+(Y/X)\tan\theta_k}\right)$$

$$=\frac{-1}{2\pi RC}\left(\frac{\sin\theta_k+\alpha\sin 2\theta_k}{\cos\theta_k+\alpha\cos 2\theta_k}\right). \tag{10}$$

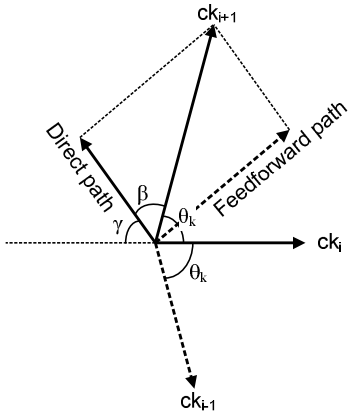


Figure 5. Phase relationship between input and output signals of the unit stage.

B. *Determining Mode Domiance*

Fig. 6 (a) and (b) show γ and |G(α)|, respectively, for each k value in a five-stage FRO. We assumed that the DC gain of the inverting amplifier used in the unit stage is 20, a typical value for a CMOS inverter. From the figure, we can determine the range of α for each k that satisfies the oscillation condition, or $0 \le \gamma < \pi/2$ and $|G(\alpha)| > 1$. In the figure, the shadowed regions represent those ranges where the oscillation condition cannot be satisfied. For example, for $0<\alpha<0.45$, only k=2 can satisfy the conditions. For $0.45<\alpha<0.6$, both k=1 and 2 can satisfy the conditions. But k=2 has much greater magnitude response, becoming the dominant mode. For $0.6<\alpha<1$, k=1 and 3 both satisfy the oscillation conditions but k=3 is the dominant mode. Finally, for $\alpha>1$, k=1 and 3 both satisfy the conditions, but k=1 is the dominant mode.

Fig. 7 (a) shows calculated the oscillation frequency of the dominant mode using (10) as α changes. For comparison, Fig. 7(b) shows SPICE-simulated oscillation frequencies. For SPICE simulation, typical CMOS inverters with 0.18μm channel length are used. For easier comparison, oscillation frequencies in each figure are normalized with $f_{5,a}=0.0363f_T$ and $f_{5,b}=3.28$GHz, the oscillation frequency of five-stage FRO with α=0, for the model-based calculation and SPICE simulation, respectively. There is a good agreement for the overall dependence of oscillation frequencies on α between two cases. In particular, those α values where the mode transition occurs are very well predicted by our model. Consequently, we can reliably use our model to determine α for the mode having desired oscillation frequency characteristics.

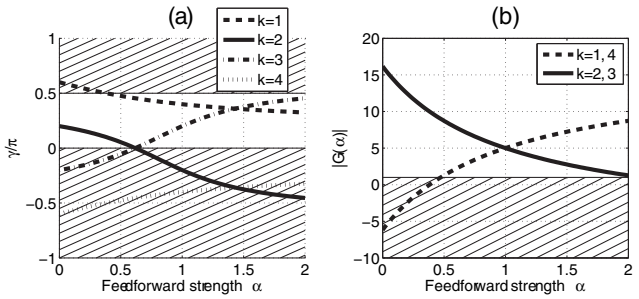


Figure 6. Five-stage FRO unit stage characteristics: (a) Normalized frequency-dependent phase response γ and (b) Magnitude response |G(α)|.

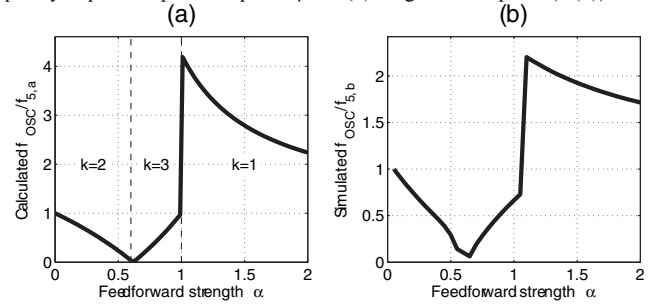


Figure 7. Comparison between model-prediction and SPICE simulation result: (a) model prediction, (b) SPICE simulation

III. FRO Frequency Maximization

Oscillation frequencies for FROs can be greatly enhanced from those for ROs as can be shown in Fig. 7. For earlier analyses, we used 20 DC gain for the inverting amplifier. Although this is a typical value for CMOS inverters, this provides much larger gain than required for oscillation. In fact, adding feed forward paths with proper strength α to ROs trades some portion of the excess gain for higher oscillation frequencies. Another way of achieving this is lowering the output resistance of the inverting amplifier using a resistor-loaded inverting amplifier as shown in Fig. 8. The DC gain dependence on the load resistance R are shown in Fig. 9. The NMOS transistor's length and width are 1μm and 0.18μm, respectably. For speed optimization, the minimum α, α_{min}, which gives an amplitude gain greater than one at the oscillation frequency can be determined from (9) as

$$\alpha_{\min}(R) = -[1 + A_{DC}\cos(\theta)]/[1 + A_{DC}\cos(2\theta)]. \quad (11)$$

Because we want the oscillator to operate in mode 1, θ is set to $2\pi/5$. From (10) using α_{min} yields the maximum oscillation frequency for given R.

The calculated maximum frequency and the corresponding α_{min} are plotted as functions of R in Fig. 9. When R is around 5KΩ, the oscillation frequency reaches its maximum value of about 17GHz. At the same time, α_{min} is found at around 2.2. Interestingly, α_{min} is much larger than the optimal value of 1 derived in the previous section. It is because a large amount of amplitude gain is traded for extra bandwidth, and the feed forward paths are scaled up to compensate lowered gain.

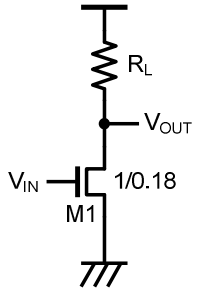


Figure 8. Resistor-loaded inverting amplifier in unit size.

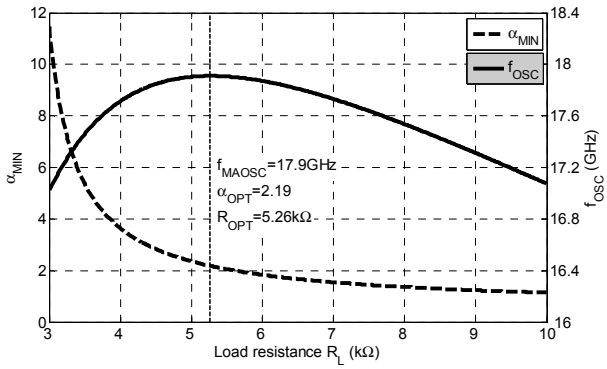


Figure 9. Calculated α_{min} for the FRO to operate with k=1 at a given R, and the oscillation frequency of the five- stage FRO.

It is shown that the oscillation frequency reaches its maximum at α_{OPT}=2.19 with R_{OPT} = 5.26kΩ. After that point, the oscillation frequency droops since f_T decreases as R_L increases.

IV. Test Chip Design and Layout

With the calculated parameters, R_{OPT} and α_{OPT}, a five-stage FRO is designed using 0.18-µm CMOS technology. Fig. 10 shows the unit stage structure of the fabricated FRO. M2 is added to the unit stage structure for stable oscillation as well as for frequency tunability.

The designed FRO layout is shown in Fig. 11. It has RF probe pads for easy measurement. ESD protection circuits are included only for VCO control voltage input to avoid any extra load capacitance.

Post-layout simulation results including pads and ESD structures are shown in Fig. 12. The FRO is degraded by 15% due to the layout parasitic components. The output signal swings of FRO are designed to be larger than 800mV$_{P2P}$ and 200mV$_{P2P}$ in the core and at the 50Ω resistor for the output buffer for the entire frequency range. The estimated power consumption is around 50mW including the output buffer transistor.

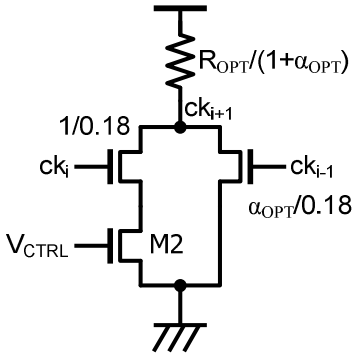


Figure 10. Unit stage structure of the designed FRO.

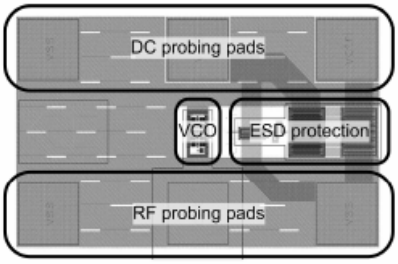


Figure 11. Microphotograph of fabricated FRO

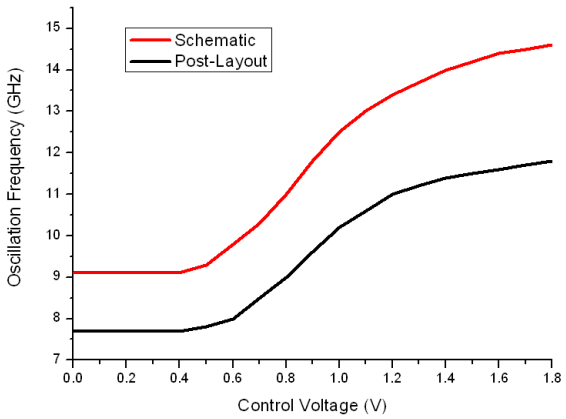


Figure 12. Measured oscillation frequency of the FRO.

V. Conclusion

In this paper, a simple linear FRO model and design equations are developed. It is shown that our model can predict FRO behaviors very accurately. In addition, five-stage FRO is optimized for the highest oscillation frequency. Resistor-loaded inverting amplifiers are used as the delay stage. Post-layout simulation results show that oscillation frequency up to 12GHz is achievable with a typical 0.18-µm CMOS process

References

[1] Seog-Jun Lee, Beomsup Kim, and Kwyro Lee, "A novel high-speed ring oscillator for muliphase clock generation using skewed delay scheme" IEEE J.Solid-State Circuits, vol. 32, no. 2, pp. 289-291, Feb. 1997

[2] Chan-Hong Park, and Beomsup Kim, "A low-noise, 900-MHz VCO in 0.6-µm CMOS", IEEE J.Solid-State Circuits, vol.34, no. 5, pp. 586-591, May 1999.

[3] Lizhong Sun, Tad Kwasniewski, and Kris Iniewski, "A quadrature output voltage controlled ring oscillator based on three-stage sub-feedback loops" in Proc. IEEE Int. Symp. Circuits Syst.(ISCAS'99), vol.2, pp. 176-197 1999

[4] M. Grozing, and M. Berroth, "CMOS ring oscillator with quadrature outputs and 100MHz to 3.5GHz tuning ragne", in proc. European Solid-State Circuits Conference(ESSCIRC'03), pp. 679-682, 2003

[5] Dean A. Badillo and Sayfe Kiaei, " A low phase noise 2.0V 900MHz CMOS voltage controlled ring oscillator", in proc. IEEE Int. Symp. Circuits Syst. (ISCAS'04), vol. 4, pp. 533-536, 2004

[6] Fadi H. Gebara, Jeremy D. Schaub, Alan J. Drake, Kevin J. Nowka, and Richard B. Brown, "4.0Ghz 0.18µm CMOS PLL based on an interpolative oscillator", in digest of technical papers, Symp. On VLSI Circuits, pp. 100-103, 2005.

[7] Hai Qi Liu, Wang Ling Goh and Liter Siek, "0.18-µm 10-GHz CMOS ring oscillator for optical transceivers", in proc. IEEE Int. Symp. Circuits Syst. (ISCAS'05), vol. 4, pp. 1525-1528, 2005.

[8] Yalcin Alper Eken and John P. Uyemura " A 5.9-GHz voltage-controlled ring oscillator in 0.18-µm CMOS", IEEE J. Solid-State Circuits, vol. 39, no. 1, pp. 230-233, Jan. 2004.

[9] E.Carin, M. H. Perrott, "A numerical design approach for high speed differential resistor-loaded, CMOS amplifiers", in proc. IEEE Int. Symp. Circuits Syst. (ISCAS'04), vol. 5, pp. 508-511, 2004.