# A-SSCC 2008

The 4th
IEEE Asian Solid-State Circuits Conference
Fukuoka, November 3-5, 2008

# Advance Program





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# A-SSCC2008 Program at a Glance

## Nov. 3

| | Navis-C | Navis-B | Navis-A | Argos-F | Argos A&B | Nire | Kusu |
|---|---|---|---|---|---|---|---|
| 09:00-10:20 (80) | Tutorial 1<br>Design of Femto-joule Energy Efficient ADCs in CMOS<br>Geert Van der Plas (IMEC) | Tutorial 2<br>Advanced SiP design<br>Joungho Kim (KAIST) | | Panel Exhibition<br>by<br>Fukuoka Industry, Science & Technology Foundation<br>(Fukuoka IST)<br><br>http://www2.lab-bt.jp/english/ | | Organizing Committee Office | Internet Lounge |
| 10:20-10:40 (20) | Break | | | | | | |
| 10:40-12:00 (80) | Tutorial 1<br>Design of Femto-joule Energy Efficient ADCs in CMOS<br>Geert Van der Plas (IMEC) | Tutorial 2<br>Advanced SiP design<br>Joungho Kim (KAIST) | | | | | |
| 12:00-13:00 (60) | Lunch | | | | | | |
| 13:00-14:20 (80) | Tutorial 3<br>Advanced Clock Distribution System<br>Simon Tam (Intel) | Tutorial 4<br>Economic and Design Choices for Nano-scale Electronic Systems<br>Siva Narendra (Tyfone) | | | | | |
| 14:20-14:40 (20) | Break | | | | | | |
| 14:40-16:00 (80) | Tutorial 3<br>Advanced Clock Distribution System<br>Simon Tam (Intel) | Tutorial 4<br>Economic and Design Choices for Nano-scale Electronic Systems<br>Siva Narendra (Tyfone) | | | | | |
| 16:00-17:30 (90) | | | | Student Design Contest (SDC) | | | |
| 17:30-19:00 (90) | Welcome Reception | | | | | | |

## Nov. 4

| | Navis-C | Navis-B | Navis-A | Argos-F | Argos A&B | Nire | Kusu |
|---|---|---|---|---|---|---|---|
| 08:30-08:40 (10) | Opening Ceremony | | | | | | |
| 08:40-08:50 (10) | Welcome Speech of Fukuoka Prefectural Governor | | | | | | |
| 08:50-09:35 (45) | Plenary Talk 1<br>"Aiming for an Environmental-Oriented CE Platform"<br>Yoshiaki Kushiki (Panasonic) | | | Panel Exhibition by Fukuoka IST | | Organizing Committee Office | Internet Lounge |
| 09:40-10:25 (45) | Plenary Talk 2<br>" Foundry-Fabless Collaboration for Semiconductor SoC Industry in Korea"<br>Young Hwan Oh (Dongbu HiTek Semiconductor) | | | | | | |
| 10:25-10:55 (30) | Break | | | SDC Exhibition | | | |
| 10:55-12:35 (100) | Industry Program 1<br>Processors and Multimedia Circuits<br>Stefan Rusu (Intel), Shaojun Wei (Phoenix Microelectronics) | Industry Program 2<br>High-Speed Signaling and Interfaces<br>Chenghyun Kim (Samsung Electronic), Koji Kai (Panasonic) | | Panel Exhibition by Fukuoka IST | | | |
| 12:35-13:40 (65) | Lunch | | | | | | |
| 13:40-15:45 (125) | Session 1<br>Multi-stage A/D Converters<br>Yong Moon (Soongsil Univ.), Koichi Ono (Sony) | Session 2<br>Power and Delay Reduction Techniques for Digital Circuits<br>Xiaoyang Zeng (Fudan Univ.), Hideyuki Kabuo (Panasonic) | Session 3<br>Short-Range Interface Systems<br>Yasumoto Tomita (Fujitsu Laboratories), Hiroyuki Mizuno (Hitachi) | Session 4<br>mm-Wave CMOS Circuits<br>Shouhei Kousai (Toshiba), Howard Luong (HKUST) | | | |
| 15:45-15:50 ( 5) | Break | | | | | | |
| 15:50-17:30 (100) | Panel Discussion 1<br>SiP2.0: What, When, and How?<br>Masayuki Mizuno (NEC Electronics) | Panel Discussion 2<br>Digitally Assisted Analog and RF Circuits: Potentials and Issues<br>Asad A. Abidi (UCLA) | | Panel Exhibition by Fukuoka IST | | | |
| 17:30-18:00 (30) | Break | | | SDC Exhibition | | | |
| 18:00-18:45 (45) | Special Lecture<br>How to Write a Good JSSC Paper<br>Bram Nauta (Univ. of Twente) | | | Panel Exhibition by Fukuoka IST | | | |
| 18:45-19:00 (15) | Break | | | | | | |
| 19:00-21:00 (120) | | | | | Banquet | | |

## Nov. 5

| | Navis-C | Navis-B | Navis-A | Argos-F | Argos A&B | Nire | Kusu |
|---|---|---|---|---|---|---|---|
| 08:30-08:15 (45) | Plenary Talk 3<br>"4G Wireless Technology: When will it Happen? What does it Offer?"<br>Bill Krenik (Texas Instruments) | | | | | | |
| 08:15-09:50 (35) | Break | | | | | | |
| 09:50-12:20 (150) | Session 5<br>Advanced Power Management<br>Yasuhiro Sugimoto (Chuo Univ.), Bill Liu (Analog Devices, Shanghai) | Session 6<br>Multimedia Signal Processing<br>Takeshi Ikenaga (Waseda Univ.) Oh-Kyong Kwon (Hanyang Univ.) | Session 7<br>Wireline Communication<br>Woo Geun Rhee (Tsinghua Univ.), Hiroyuki Okada (NEC Electronics) | Session 8<br>Memory<br>Hiroyuki Yamauchi (Fukuoka Inst. of Tech.), Jae-Yoon Sim (POSTECH) | | Organizing Committee Office | Internet Lounge |
| 12:20-13:20 (60) | Lunch | | | | | | |
| 13:20-15:25 (125) | Session 9<br>Analog Circuit Technique<br>Sung Min Park (Ewha Womans Univ.), Tsung-Hsien Lin (National Taiwan Univ.) | Session 10<br>Communication Signal Processing<br>Ramchan Woo (LG Electronics), Tai-cheng Lee (National Taiwan University) | Session 11<br>Electronics for Health<br>Ali Keshavarzi (TSMC), Reiji Hattori (Kyushu Univ.) | Session 12<br>RF Transceiver Circuits<br>Kang-Yoon Lee (Konkuk Univ.), Ryangsu Kim (Panasonic) | | | |
| 15:25-15:45 (20) | Break | | | | | | |
| 15:45-18:15 (150) | Session 13<br>Sigma-Delta and Flash Data Converters<br>Hung-Sung Li (MediaTek), Satoku Tsukamoto (Fujitsu Laboratories) | Session 14<br>Measurement & Characterization of Digital Circuits<br>Makoto Ikeda (Univ. of Tokyo), Vasanthe Ereguntla (Intel Technology India) | Session 15<br>Clock Generation Circuits<br>Srikanth Gondi (K-Micro America), Koichiro Mashiko (Renesas Technology) | Session 16<br>RF Amplifiers and VCOs<br>Minoru Fujishima (Univ. of Tokyo), Hyunchol Shin (Kwangwoon Univ.) | | | |

## Session 12 : RF Transceiver Circuits

Time: 13:20-15:25
Room: Arogs F

Co-Chairs: Kang-Yoon Lee (Konkuk University)
Ryangsu Kim (Panasonic)

### 12-1 13:20-13:45

**A World-Band Triple-Mode 802.11a/b/g SOC in 0.13um CMOS**

Chia-Hsin Wu, Yuan-Hung Chung, Anson Lin, Wei-Kai Hong, Jie-Wei Lai, Cheng-Yu Wang, Chih-Hsien Shen, Yu-Hsin Lin, Yi-Hsien Cho, Yang-Chuan Chen
*MediaTek Inc., Taiwan*

*Abstract*- A world-band triple-mode SOC compliant with 802.11a/b/g is realized in 0.13μm CMOS technology. This SOC features multiple integrated capless LDOs to be compatible with DC/DC supply for low current consumption and minimizing external BOMs. With supplying by a DC/DC converter, the measured 2.4GHz/5GHz sensitivity is -77.5dBm/-74dBm at 54Mbps, and TX 2.4GHz/5GHz 54Mbps EVM is -32dB/-30dB at an output power of -7dBm/-8dBm. This SOC consumes 71mA/83mA at RX mode and 56mA/74mA at TX mode at 2.4GHz/5GHz band respectively.

### 12-2 13:45-14:10

**A 52 pJ/bit OOK Transmitter with Adaptable Data Rate**

M.Kumarasamy Raja and Yong Ping Xu
*National University of Singapore, Singapore*

*Abstract*- A 433-MHz OOK transmitter with adaptable data rate is presented. The proposed circuit completely turns off the transmitter during the transmission of '0' and employs a speed-up scheme to obtain high data rates and low wake up time. The data rate can be adjusted and adapted to the need of applications. Realized in a 0.35-μm CMOS technology, the OOK transmitter has a measured output power of -12.7dBm with a dc power consumption of 560 μW under a 1-V power supply, and a data rate of 3 Mb/s, yielding an energy efficiency of 187 pJ/bit or 3.48 nJ/bit/mW if normalized to the transmitting power. When the proposed speed-up circuitry is enabled, data rate increases to 10 Mb/s, with a dc power consumption of 518 μW achieving an energy efficiency of 52 pJ/bit or 0.97 nJ/bit/mW when normalized.



### 12-3 14:10-14:35

**A 1.2V Interference-Sturdiness, DC-Offset Calibrated CMOS Receiver Utilizing a Current-Mode Filter for UWB**

Horng-Yuan Shih[1], Wei-Hsien Chen[2], Kai-Chenug Juang[2], Tzu-Yi Yang[2], Chien-Nan Kuo[1]
*1) National Chiao-Tung University, Taiwan*
*2) Industrial Technology Research Institute, Taiwan*

*Abstract*—An interference-sturdiness receiver with a currentmode filter for 3-5GHz UWB applications is implemented in a 1.2V 0.13μm CMOS process. The chip provides a maximum voltage gain of 70dB and a dynamic range of 60dB. The measured in-band OIP3 is +9.39dBm, out-of-band IIP3 -15dBm and noise figure 6.8dB in the maximum gain mode. An algorithm for the automatic digital DC offset calibration is also demonstrated.

### 12-4 14:35-15:00

**A Programmable-Bandwidth Front-End with Clock-Interleaving Down-Conversion Filters**

Ming-Feng Huang, and Lai-Fu Chen
*Industrial Technology Research Institute, Taiwan*

*Abstract*—Integration of a programmable-bandwidth frontend (PBFE) based on clock-interleaving down-conversion filter (CIDCF) is presented. After demonstration, PBFE has a programmable bandwidth from 1-MHz to 110-MHz. Under 6.14- mA power current (excluding output buffer) and 1.2-V power supply, PBFE gets +8.2-dBm $IIP_3$, +45-dBm $IIP_2$ and 2.6-dB gain. Moreover, a better than 30.59-dB alias-band rejection and 34.032-dB image rejection ratio are obtained. Using a 64- QAM signal with 54-MS/s for IEEE 802.11g standard, PBFE achieves -26.351-dB EVM on a 2.412-GHz RF frequency, 1.072-GHz LO frequency, and 1072-MS/s sampling frequency.

### 12-5 15:00-15:12

**A 1.8-V CMOS Direct-Conversion Tuner for Mobile DTV Applications**

Fei Song, Huailin Liao, Jiang Chen, Le Ye, Huaizhou Yang, Junhua Liu, Jinshu Zhao, Ru Huang
*Peking University, China*

*Abstract* -A 1.8-V 0.18μm CMOS direct-conversion Tuner for UHF band mobile digital TV applications is presented. To meet the stringent requirements of Noise Figure (NF) and IIP3, a capacitor cross-coupled (CCC) common-gate LNA and a novel high-linearity, low-flicker noise Gilbert Mixer are adopted. The LNA achieves 26dB variable gain by using digital controlled current-steering technique and a resistive attenuator. To overcome the gain roll-off at the high frequency channels, a current reuse self-biased post-LNA buffer is proposed as the interface between the VGLNA and Mixer. In addition, a fully integrated DC Offset Correction (DCOC) circuit with switchable high-pass corner frequency, is introduced to realize both low high-pass cutoff frequency and short settling time. A wideband integer-N synthesizer using an adaptive frequency calibration (AFC) of dichotomizing technique, settles less than 200μs for LO generation. The tuner achieves 3.8dB NF, 0dBm IIP3@20dB LNA gain attenuation, 92dB gain dynamic range and occupies 3.45mm× 3.4mm silicon area, while drawing 59mA from 1.8-V voltage supply.

## 12-6 15:12-15:24

**1-Gb/s Mixed-Mode BPSK Demodulator Using a Half-Rate Linear Phase Detector for 60-GHz Wireless PAN Applications**

Kwang-Chun Choi, Duho Kim, Minsu Ko and Woo-Young Choi
*Yonsei University, Korea*

*Abstract*- A mixed-mode high-speed binary phase-shift keying (BPSK) demodulator for IEEE802.15.3c mm-wave wireless personal area network (WPAN) application is realized with 0.18μm CMOS process. The demodulator core consumes 23.4 mW from 1.8 V power supply while the chip area is 165 × 110 $\mu m^2$. The power-consumption is less than that of the conventional BPSK demodulators and the chip-size is smaller. The proposed circuit is verified by 1-meter 60-GHz wireless link tests with 1-Gb/s data.



# Session 13 : Sigma-Delta and Flash Data Converters

Time: 15:45-18:15
Room: Navis C

Co-Chairs: Hung S. Li (Mediatek)
Sanroku Tsukamoto (Fujitsu Laboratories)

## 13-1 15:45-16:10

**A 2.4GHz 40mW 40dB SNDR/62dB SFDR 60MHz Bandwidth Mirrored-Image RF Bandpass ΣΔ ADC in 90nm CMOS**

Julien Ryckaert[1], Jonathan Borremans[1,2], Bob Verbruggen[1,2], Joris Van Driessche[1], Liesbet Van der Perre[1], Jan Craninckx[1] and Geert Van der Plas[1]
*1) IMEC, Belgium*
*2) Vrije Universiteit Brussel, Belgium*

*Abstract*—A 6th order RF bandpass ΣΔ ADC operating on the 2.4GHz ISM band is presented. The bandpass loop filter is based on digitally programmable Gm-LC resonators. By using a mirrored-image sampling technique, the clock frequency is reduced to 3GS/s, thereby reducing the power consumption. Implemented in a standard 90nm CMOS process, the IC achieves 40dB and 62dB of SNDR and SFDR respectively on a 60MHz bandwidth with 40mW of power consumption.

## 13-2 16:10-16:35

**A 350-MHz Combined TDC-DTC with 61 ps Resolution for Asynchronous ΔΣ ADC Applications**

Jorg Daniels[1], Wim Dehaene[1], Michiel Steyaert[1], Andreas Wiesbauer[2]
*1) Katholieke Universiteit Leuven, ESAT-MICAS, Belgium*
*2) Infineon Technologies AG, Austria*

*Abstract*—A combined Time-to-Digital Digital-to-Time Converter (TDC-DTC) is presented for use in a high-precision single-bit Asynchronous ΔΣ ADC. It quantizes the 1-bit asynchronous square wave with 61 ps precision, obtaining a virtual sampling frequency of 16.4 GHz with only a 350 MHz clock. Measurements confirm that with this precision, the design of a single-bit Asynchronous ΔΣ ADC obtaining 78 dB SNDR over a 500 kHz bandwidth is feasible using only a first-order noise shaping and with a limit cycle frequency of only 8 MHz. With this technique, both the order and the bandwidth requirements of the noise shaping filter can be relaxed, which significantly reduces the analog complexity of the ΔΣ Modulator. The proposed architecture is therefore especially suited for low-voltage nanometer technologies.

# 1-Gb/s Mixed-mode BPSK Demodulator Using a Half-rate Linear Phase Detector for 60-GHz Wireless PAN Applications

Kwang-Chun Choi, Duho Kim, Minsu Ko and Woo-Young Choi

Department of Electrical and Electronic Engineering

Yonsei University

Seoul, Korea

c3kc@tera.yonsei.ac.kr

***Abstract*- A mixed-mode high-speed binary phase-shift keying (BPSK) demodulator for IEEE802.15.3c mm-wave wireless personal area network (WPAN) application is realized with 0.18μm CMOS process. The demodulator core consumes 23.4 mW from 1.8 V power supply while the chip area is 165 × 110 μm$^2$. The power-consumption is less than that of the conventional BPSK demodulators and the chip-size is smaller. The proposed circuit is verified by 1-meter 60-GHz wireless link tests with 1-Gb/s data.**

## I. Introduction

The unlicensed 60-GHz band provides opportunities for the wireless personal area network (WPAN) application and there are on-going standardization efforts for this application [1]. 60-GHz offers wide bandwidth (7-GHz), and Gb/s data transmission is possible. Two kinds of baseband modems, single carrier and orthogonal frequency-division multiplexing (OFDM) modems, are discussed in the standardization. Single carrier modems are easier to implement, because their structure is simpler and requires less power-amp linearity than OFDM modems. Although the multi-path fading effect is a problem for single-carrier links, the use of directional antennas can ease the burden [2].

In digital single-carrier demodulators, the speed of analog-to-digital converter (ADC) limits the maximum symbol rate. Digital interpolation [3], which is the most popular digital approach, needs GSamples/s ADC to sample Gsymbol/s signal, and its realization with CMOS is not an easy task. A mixed-mode baseband demodulator can ease this burden [4]. A mixed-mode binary phase-shift keying (BPSK) demodulator having a small chip-size and low power-consumption was reported for home-network applications [5]. An improved version of the demodulator and its application for 60-GHz WPAN is demonstrated in this paper.

This paper is organized as follows. Section II explains the mixed-mode approach to BPSK demodulator. Section III proposes an improved mixed-mode BPSK demodulator circuit. Section IV verifies the designed chip at 1-Gb/s data-rate with 1-meter 60-GHz wireless link tests.

We acknowledge the support IC Design Education Center (IDEC) for supplying CAD tools used in our research.

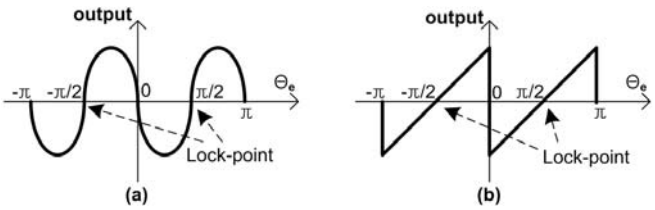


Fig. 1. Phase detection characteristics: (a) Costas-loop (b) half-rate linear phase detector

## II. Mixed-mode Approach

If BPSK modulated signal is supplied to the Costas-loop, the phase difference (=sin2$\theta_e$) between input signal and internal clock is generated. This process is similar to the phase detection process in phase-locked loop (PLL) or clock-data recovery (CDR) circuits. Consequently, a BPSK demodulator can be realized with the phase-locking architecture.

The phase-detection characteristics of the Costas-loop are shown in Fig. 1(a). Because BPSK signals have two phases, there should be two lock-points at π/2 and -π/2 rad. This feature can be realized by a half-rate linear phase-detector (PD), which is generally used for CDR circuits, and its phase-detection characteristics are shown in Fig. 1(b).

The BPSK modulated signals (MOD) can be represented as

$$MOD = DATA \times \sin\omega_C t,$$

where DATA represents input data having 1 for 'high (H)' and -1 for 'low (L)', and $\omega_C$ is the carrier frequency. Fig. 2 shows 2-symbols of BPSK signals in the time domain. Slicing them with a hard limiter produces signal shapes very similar to baseband NRZ data. This means that CDR circuits for NRZ data can be applied for synchronizing demodulator clocks to BPSK carrier signals. As shown in the figure, each sequence consists of 2-bit NRZ data in which the front bit is identical to the input symbol.

The demodulator frequency is desired to be the same as the carrier frequency. For BPSK signals, there are 2-bit NRZ data

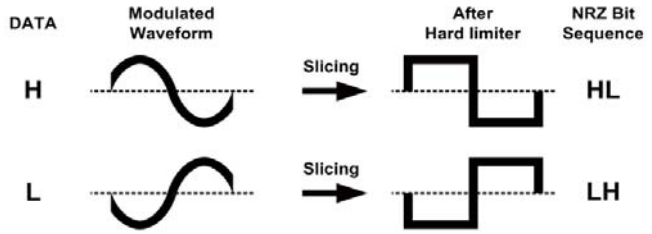


Fig. 2. Mixed-mode approach

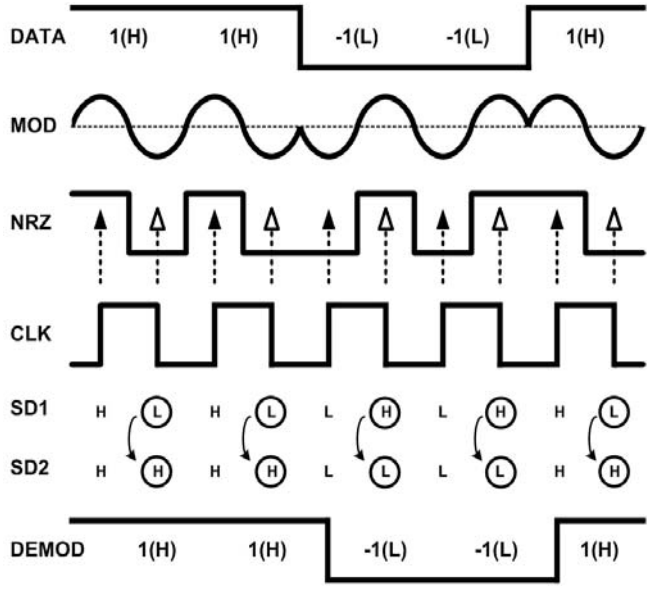


Fig. 3. Data detection flow

within one period of carrier signals. Consequently, half-rate CDR, which uses 1/2 frequency of the data rate, is used.

Fig. 3 shows the data detection flow with a half-rate CDR. The modulated signal, MOD, changes its phase at transition edges of DATA. A hard limiter makes modulated signals into NRZ sequences. After synchronization, the demodulator clock, CLK, is aligned as shown in the figure. SD1 represents the sampled data at both rising and falling edges of CLK. Data detection (DEMOD) can be achieved by inverting all the bits of SD1 that are sampled at the falling edges of CLK (shown as SD2 in the figure).

With this scheme, a BPSK demodulator can be implemented without ADC. For high speed conversion, most ADCs use the flash structure. An n-bit flash ADC requires $2^n$ comparators, $2^n$ S&H circuits, a reference generator, and a $2^n$-bit decoder. In contrast, our scheme is basically based on one-bit sampler. Consequently, the proposed demodulation scheme consumes less power and occupies smaller area than the digital interpolation scheme which employs ADC and additional digital logic circuits.

## III. An Improved BPSK Demodulator Circuit

The bang-bang PD employed in [5] has an advantage for high-speed operation, but the recovered clock has large jitters because the PD gain is very large [6]. In addition, it requires the use of quadrature clock signals, which often causes the mismatch problem between two clock signals.

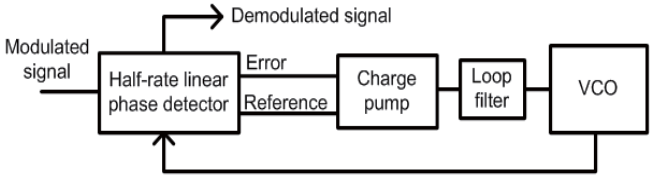


Fig. 4. Block diagram of proposed circuit

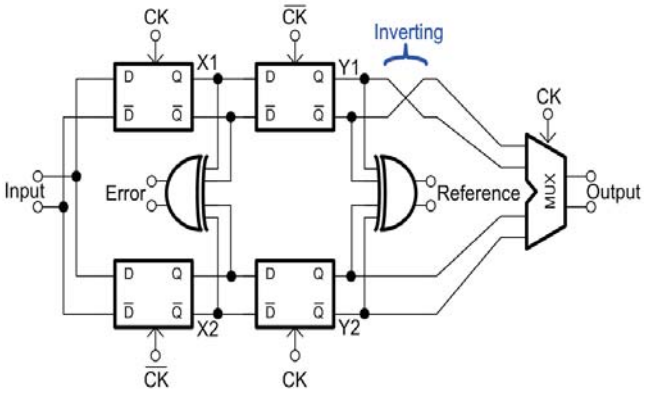


Fig. 5. Block diagram of half-rate linear PD with BPSK demodulating function

We propose a new BPSK demodulator having an improved PD architecture. The block diagram is shown in Fig. 4. It is very similar to an analog half-rate CDR circuit. Demodulating function is realized by a few modification of the PD architecture. The block diagram for PD is shown in Fig. 5, which is based on the structure given in [6]; except that Y1 representing the sampled bits by the falling edge of clock is inverted. This PD is composed of 4 latches, 1 MUX and 2 XOR gates. Moreover, this PD does not require quadrature clocks for half-rate operation. Thus it is much simpler than the PD used in [5]. For the VCO in the demodulator, a differential -ended 4-stage ring oscillator [7] is used.

Because the structure of designed BPSK demodulator is similar to that of conventional analog PLL-based CDR, loop-dynamics can be analyzed by conventional equations; except that the PD gain is different from that in conventional CDR analysis. The error-transfer function can be represented as

$$H_e(s,N) = \frac{s}{s + K_{PD}(N) \cdot I_{CP} \cdot F(s) \cdot K_{VCO}}$$

where $I_{CP}$ is the charging current(A), F(s) is the impedance of loop-filter, $K_{VCO}$ is the gain of VCO(rad $s^{-1}V^{-1}$), and $K_{PD}(N)$

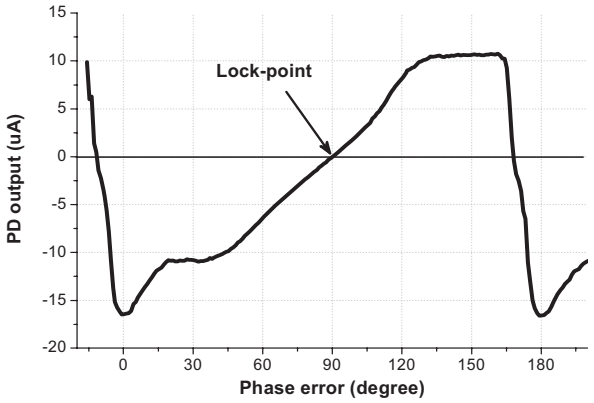


Fig. 6. Simulated characteristic of PD with charge-pump

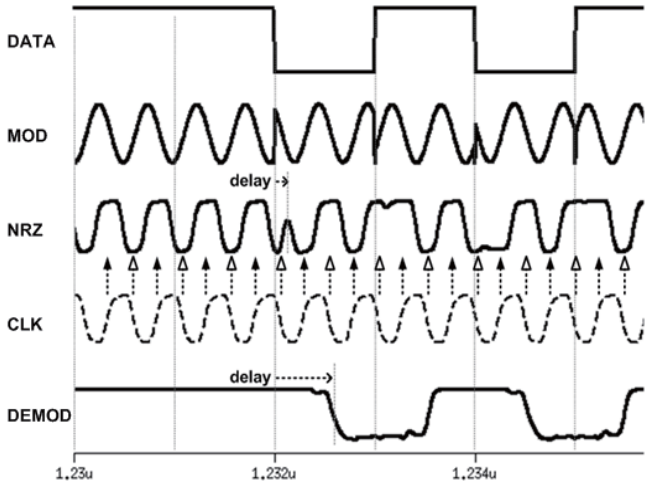


Fig. 7. Simulation result of designed circuit

is the gain of PD which depends on the frequency-ratio, N, between carrier frequency and data-rate of BPSK-modulated signal. When N is equal to 2, for instance, the $K_{PD}$ can be approximated to $7/4\pi$. With large N, the $K_{PD}$ goes close to $2/\pi$.

Simulated PD characteristic with charge-pump is shown in Fig. 6. For this simulation, $I_{CP}$ is set to 20μA, and BPSK signals are generated with 2.05-GHz carrier and 1-GSymbol/s data. The average of output current is measured as a function of input phase difference. The simulation result shows that the PD is linear over 105-degrees, and has one lock-point within 180-degrees. The slope of the curve around the lock-point, $K_{PD}$, is about $34.2\mu A/\pi$. It is well-matched to $7/4\pi \times 20\mu A$, which is calculated value with N=2.

Fig. 7 shows the simulation result of designed demodulator circuit with 1-Gb/s data-rate and 2.05-GHz carrier-frequency.

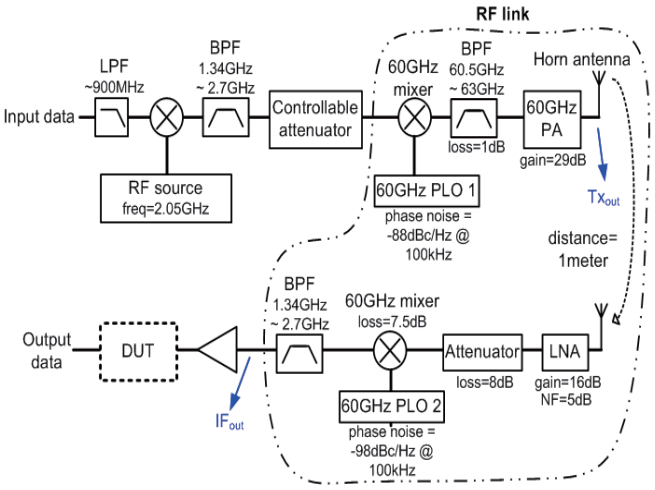


Fig. 8. Measurement setup with 60-GHz wireless link

## IV. Measurements

The demodulator is fabricated with 0.18μm CMOS technology. The measurement setup is shown in Fig. 8. The BPSK signals are generated by mixing $2^7$-1 pseudo-random binary sequence (PRBS) data with 2.05-GHz local oscillator signal. RF filters are used to realize the band-limited channel. A tunable attenuator is used to measure the BER vs. SNR performance. 60-GHz RF link is composed of commercial RF components. The distance between Tx and Rx is 1-meter in accordance with the usage model 5 of IEEE 802.15.3c [1]. The signal-loss from $Tx_{out}$ node to $IF_{out}$ node is -19.6 dB. This is due to the insertion loss about 8 dB between 60-GHz LNA and 60-GHz Rx mixer. In order to satisfy the required input swing of DUT, IF-amplifier and limiting amplifier are used in front of DUT.

At first, measurement with the back-to-back link in which $IF_{out}$ node is directly connected to the attenuator, is done. With $IF_{out}$ power larger than -38.5 dBm, the demodulator operates without any errors for 1-Gb/s data. The measured BER at different $IF_{out}$ powers is shown in Fig. 10.

The fabricated chip is also tested with a 60-GHz wireless link. With the wireless link, the demodulator operates without any errors for 1-Gb/s data if $IF_{out}$ power is larger than -36 dBm. The eye diagram of demodulated signals in the error-free condition is shown in Fig. 9 and the phase noise of the recovered clock is shown in Fig. 10. BER vs. $IF_{out}$ power is also measured and the results are shown in Fig. 11. The wireless link causes about 7.5 dB penalty at $10^{-9}$ BER. The reason for the difference in BER slopes between back-to-back and wireless links is not clear at the moment and further investigations are being done. Table I summarizes the performance of the fabricated chip.

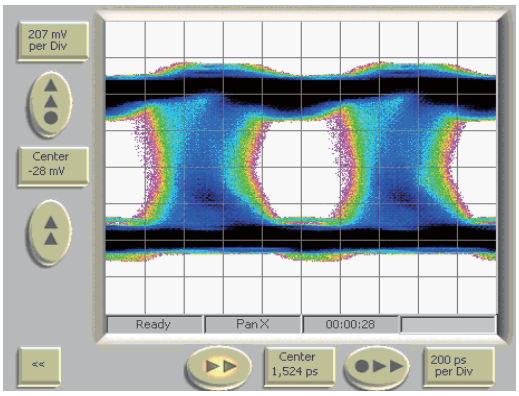


Fig. 9. Eye diagram of demodulated signal with wireless link

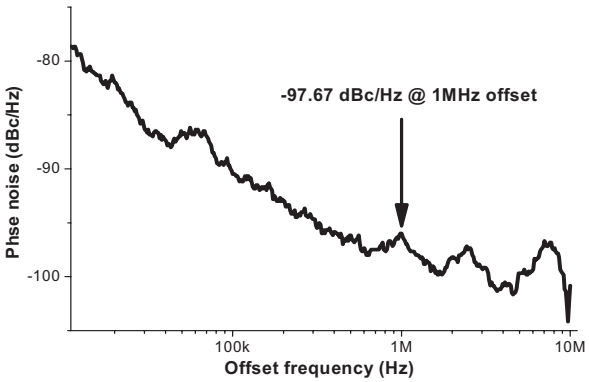


Fig. 10. Phase noise of the recovered clock

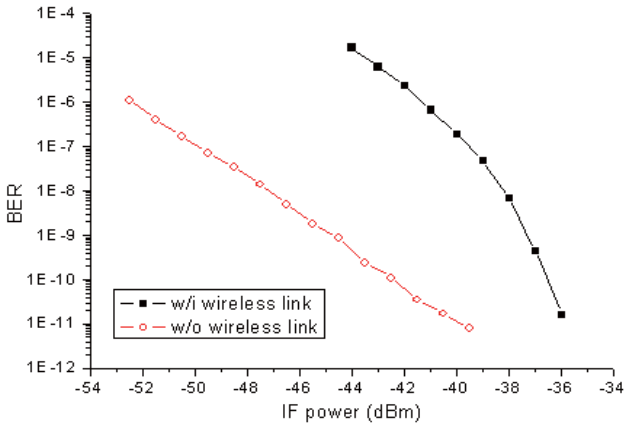


Fig. 11. BER vs. $IF_{out}$ power curve

TABLE I
PERFORMANCES OF PROPOSED CHIP

| | |
|---|---|
| **Process** | 0.18 μm |
| **Supply Voltage** | 1.8 V |
| **Carrier Frequency** | 2.05 GHz |
| **Maximum data rate** | 1 Gb/s |
| **Power Consumption** | 23.4 mW (core only) |
| **Chip Area** | 165 x 110 $\mu m^2$ (core only) |
| **Phase Noise of Recovered Clock** | -97.67 dBc/Hz @ 1MHz offset |

## V. CONCLUSION

A mixed-mode BPSK demodulator for IEEE802.15.3c millimeter-wave WPAN applicaton is demonstrated. It is fabricated with CMOS 0.18μm process and it can demodulate up to 1-Gb/s BPSK data with 2.05-GHz carrier frequency through 60-GHz wireless link. The demodulator requires small power-consumption and small chip-size as compared with conventional schemes.

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