분과	포스터세션 LIVE CHAT 일정
A. Interconnect & Package	26일(수), 09:00-11:00
B. Patterning	26일(수), 09:00-11:00
C. Material Growth & Characterization	26일(수), 14:00-16:00
D. Thin Film Process Technology	25일(화), 09:00-11:00
E. Compound Semiconductors	25일(화), 16:00-18:00
F. Silicon and Group-IV Devices and Integration Technology	25일(화), 09:00-11:00
G. Device & Process Modeling, Simulation and Reliability	25일(화), 16:00-18:00
H. Display and Imaging Technologies	25일(화), 09:00-11:00
I. MEMS & Sensors Systems	25일(화), 16:00-18:00
J. Nano-Science & Technology	26일(수), 14:00-16:00
K. Memory (Design & Process Technology)	26일(수), 14:00-16:00
L. Analog Design	26일(수), 09:00-11:00
M. RF and Wireless Design	26일(수), 14:00-16:00
N. VLSI CAD	26일(수), 09:00-11:00
O. System LSI Design	26일(수), 09:00-11:00
P. Device for Energy (Solar Cell, Power Device, Battery, etc.)	26일(수), 09:00-11:00
Q. Metrology, Inspection, Analysis, and Yield Enhancement	26일(수), 15:30-17:30
R. Semiconductor Software	26일(수), 09:00-11:00
S. Chip Design Contest	
T. AI	26일(수), 09:00-11:00
U. Bio-Medical	26일(수), 14:00-16:00

2022년 1월 26일(수), 09:00-10:30
Room F (스페이드 I, 6층)

G. Device & Process Modeling, Simulation and Reliability 분과
[WF1-G] Memory Devices and Advanced Modeling

좌장: 나현철 상무(DB 하이텍), 김성호 교수(세종대학교)

WF1-G-1 **09:00-09:15**	**Analysis of Short-Term Retention in 3-D NAND Flash Memory Using Charge Control Pulse Scheme** Donghwi Kim[1], GilSang Yoon[1], DongHyun Go[1], Junghun Park[1], Jungsik Kim[2], and Jeong-Soo Lee[1] *[1]Department of Electrical Engineering, POSTECH, [2]Division of Electrical Engineering, Gyeongsang National University*
WF1-G-2 **09:15-09:30**	**Scaling Analysis of NbO_x-Threshold Switching Devices** Hyun Wook Kim[1,2], Sol Jin[2], Heebum Kang[1], Eun Ryeong Hong[1,2], and Jiyong Woo[1,2] *[1]School of Electronic and Electrical Engineering, Kyungpook National University, [2]School of Electronics Engineering, Kyungpook National University*
WF1-G-3 **09:30-09:45**	**Variation of Electrical and Memory Characteristics of Non-Circular Cell in 3D-NAND Flash Memory** DongHyun Go[1], GilSang Yoon[1], Jounghun Park[1], Dongwhi Kim[1], Jungsik Kim[2], and Jeong-Soo Lee[1] *[1]Department of Electrical Engineering, POSTECH, [2]Division of Electrical Engineering, Gyeongsang National University*
WF1-G-4 **09:45-10:00**	**Accurate Implementation of the Bernoulli Function for the Scharfetter-Gummel Scheme** Jeong-Hyeon Do and Sung-Min Hong *School of Electrical Engineering and Computer Science, GIST*
WF1-G-5 **10:00-10:15**	**Physicochemical modeling of conformal coating on periodical high aspect ratio porous media via atomic layer deposition** Nhat-Minh Phung[1,2], Sun-Young Park[1,3], Minh-Tan Ha[1,2], Soonil Lee[2], Se-Hun Kwon[3], and Seong Min Jeong[1] *[1]Energy Efficiency Materials Center, KICET, [2]Department of Materials Science and Engineering, Changwon National University, [3]School of Materials Science and Engineering, Pusan National University*
WF1-G-6 **10:15-10:30**	**TCAD Analysis of Single-Photon Avalanche Diodes in CMOS Technology** Won-Yong Ha[1], Woo-Young Choi[1], and Myung-Jae Lee[2] *[1]Department of Electrical and Electronic Engineering, Yonsei University, [2]Post-Silicon Semiconductor Institute, KIST*

TCAD Analysis of Single-Photon Avalanche Diodes in CMOS Technology

Won-Yong Ha[1], Woo-Young Choi[1,*], and Myung-Jae Lee[2,*]

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[2]*Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology, Korea*

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The single-photon avalanche diodes (SPADs) are recently having much attention in many fields, from ranging technologies such as light detection and ranging (LiDAR) and space navigation to biomedical applications [1]. For such applications, SPADs fabricated in standard complementary metal-oxide-semiconductor (CMOS) technology have significant advantages in terms of cost and integration capability with other electrical components on the same chip. Therefore, various researches have been conducted to find the optimized CMOS-SPAD structure, especially to achieve high sensitivity at near-infrared region (NIR) where ranging technologies are interested. In order to realize the optimized CMOS-SPAD for ranging technologies, accurate device simulation is essential. In this paper, we present two different structures of CMOS-SPAD: based on a shallow junction and deep junction. By using Synopsys Sentaurus technology computer-aided design (TCAD), two CMOS-SPADs are analyzed in terms of E-field profiles and I-V characteristics. Moreover, the breakdown probabilities of the CMOS-SPADs are also investigated to optimize the device structure further.

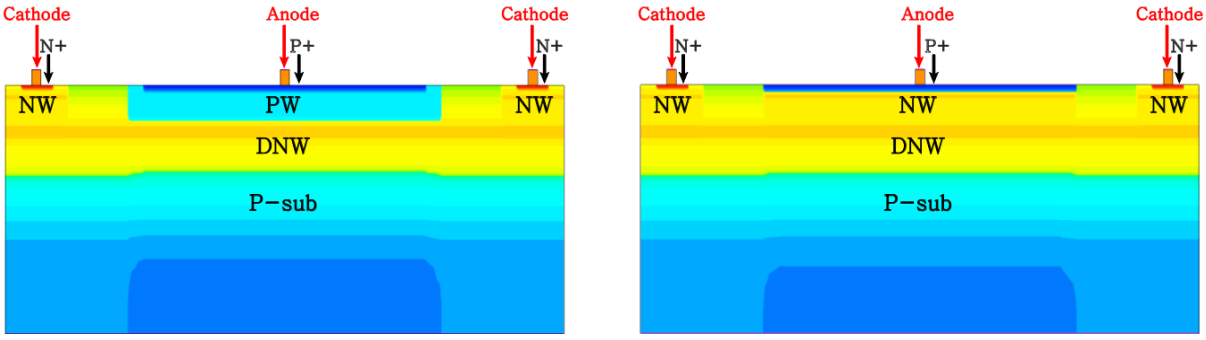

Fig 1. Cross-sections of CMOS-SPADs: (a) with shallow active junction and (b) with deep active junction

References

[1] Myung-Jae Lee and Edoardo Charbon, "Progress in single-photon avalanche diode image sensors in standard CMOS: From two-dimensional monolithic to three-dimensional-stacked technology," *Japanese Journal of Applied Physics*, (2018).