

THE 29TH KOREAN CONFERENCE ON SEMICONDUCTORS

## 제 29회 한국반도체학술대회

2022. 1. 24(월) - 26(수)

강원도 하이원 그랜드호텔(컨벤션타워) **Online & Offline Hybrid**

제 29회 한국반도체학술대회가 온/오프라인 하이브리드로 개최될 예정입니다. 제 29회 한국반도체학술대회 조직위원회와 사무국은 현장 참가자의 안전을 위해 코로나19 방역 지침에 따라 일자 별 현장 참석 인원을 선착순으로 제한합니다.

현장에 참여 예정이신 참가자께서는 참석 인원 초과 시, 숙소 등 행사장 이외의 공간에서 온라인으로 참석하실 수 있으니 본 학술대회가 안전하게 마무리 될 수 있도록 적극 협조 부탁드립니다.

(\*\* 방역 당국의 지침에 따라 변동 될 수 있습니다)

개회식 & 기초강연 유튜브 ▶

현장참가자 코로나19 대응지침 ▶

**ONLINE LIVE STREAMING**

**개회식**  
1월 25일(화) 13:50-14:00

**기초강연**

기초강연1 / 1월 25일(화) 14:00-14:50  
Memristive Neuromorphic Technology  
강성모 교수 (UC산디에이코)

기초강연2 / 1월 25일(화) 15:00-15:50  
인공지능과 반도체: 새로운 일상의 기반  
최기영 전 과기장총무장관 (서울대학교 (영예교수))



분과	포스터세션 LIVE CHAT 일정
A. Interconnect & Package	26일(수), 09:00-11:00
B. Patterning	26일(수), 09:00-11:00
C. Material Growth & Characterization	26일(수), 14:00-16:00
D. Thin Film Process Technology	25일(화), 09:00-11:00
E. Compound Semiconductors	25일(화), 16:00-18:00
F. Silicon and Group-IV Devices and Integration Technology	25일(화), 09:00-11:00
<b>G. Device &amp; Process Modeling, Simulation and Reliability</b>	<b>25일(화), 16:00-18:00</b>
H. Display and Imaging Technologies	25일(화), 09:00-11:00
I. MEMS & Sensors Systems	25일(화), 16:00-18:00
J. Nano-Science & Technology	26일(수), 14:00-16:00
K. Memory (Design & Process Technology)	26일(수), 14:00-16:00
L. Analog Design	26일(수), 09:00-11:00
M. RF and Wireless Design	26일(수), 14:00-16:00
N. VLSI CAD	26일(수), 09:00-11:00
O. System LSI Design	26일(수), 09:00-11:00
P. Device for Energy (Solar Cell, Power Device, Battery, etc.)	26일(수), 09:00-11:00
Q. Metrology, Inspection, Analysis, and Yield Enhancement	26일(수), 15:30-17:30
R. Semiconductor Software	26일(수), 09:00-11:00
S. Chip Design Contest	
T. AI	26일(수), 09:00-11:00
U. Bio-Medical	26일(수), 14:00-16:00



# 제 29회 한국반도체학술대회

The 29th Korean Conference on Semiconductors

2022년 1월 24일(월)~ 26일(수) | 강원도 하이원 그랜드호텔(컨벤션타워)

2022년 1월 26일(수), 09:00-10:30

Room F (스페이스 I, 6층)

## G. Device & Process Modeling, Simulation and Reliability 분과 [WF1-G] Memory Devices and Advanced Modeling

좌장: 나현철 상무(DB 하이텍), 김성호 교수(세종대학교)

<b>WF1-G-1</b> 09:00-09:15	<b>Analysis of Short-Term Retention in 3-D NAND Flash Memory Using Charge Control Pulse Scheme</b> Donghui Kim <sup>1</sup> , GilSang Yoon <sup>1</sup> , DongHyun Go <sup>1</sup> , Junghun Park <sup>1</sup> , Jungsik Kim <sup>2</sup> , and Jeong-Soo Lee <sup>1</sup> <sup>1</sup> Department of Electrical Engineering, POSTECH, <sup>2</sup> Division of Electrical Engineering, Gyeongsang National University
<b>WF1-G-2</b> 09:15-09:30	<b>Scaling Analysis of NbO<sub>x</sub>-Threshold Switching Devices</b> Hyun Wook Kim <sup>1,2</sup> , Sol Jin <sup>2</sup> , Heebum Kang <sup>1</sup> , Eun Ryeong Hong <sup>1,2</sup> , and Jiyong Woo <sup>1,2</sup> <sup>1</sup> School of Electronic and Electrical Engineering, Kyungpook National University, <sup>2</sup> School of Electronics Engineering, Kyungpook National University
<b>WF1-G-3</b> 09:30-09:45	<b>Variation of Electrical and Memory Characteristics of Non-Circular Cell in 3D-NAND Flash Memory</b> DongHyun Go <sup>1</sup> , GilSang Yoon <sup>1</sup> , Joungun Park <sup>1</sup> , Donghui Kim <sup>1</sup> , Jungsik Kim <sup>2</sup> , and Jeong-Soo Lee <sup>1</sup> <sup>1</sup> Department of Electrical Engineering, POSTECH, <sup>2</sup> Division of Electrical Engineering, Gyeongsang National University
<b>WF1-G-4</b> 09:45-10:00	<b>Accurate Implementation of the Bernoulli Function for the Scharfetter-Gummel Scheme</b> Jeong-Hyeon Do and Sung-Min Hong School of Electrical Engineering and Computer Science, GIST
<b>WF1-G-5</b> 10:00-10:15	<b>Physicochemical modeling of conformal coating on periodical high aspect ratio porous media via atomic layer deposition</b> Nhat-Minh Phung <sup>1,2</sup> , Sun-Young Park <sup>1,2</sup> , Minh-Tan Ha <sup>1,2</sup> , Soonil Lee <sup>2</sup> , Se-Hun Kwon <sup>2</sup> , and Seong Min Jeong <sup>1</sup> <sup>1</sup> Energy Efficiency Materials Center, KICET, <sup>2</sup> Department of Materials Science and Engineering, Changwon National University, <sup>3</sup> School of Materials Science and Engineering, Pusan National University
<b>WF1-G-6</b> 10:15-10:30	<b>TCAD Analysis of Single-Photon Avalanche Diodes in CMOS Technology</b> Won-Yong Ha <sup>1</sup> , Woo-Young Choi <sup>1</sup> , and Myung-Jae Lee <sup>2</sup> <sup>1</sup> Department of Electrical and Electronic Engineering, Yonsei University, <sup>2</sup> Post-Silicon Semiconductor Institute, KIST

# TCAD Analysis of Single-Photon Avalanche Diodes in CMOS Technology

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The single-photon avalanche diodes (SPADs) are recently having much attention in many fields, from ranging technologies such as light detection and ranging (LiDAR) and space navigation to biomedical applications [1]. For such applications, SPADs fabricated in standard complementary metal-oxide-semiconductor (CMOS) technology have significant advantages in terms of cost and integration capability with other electrical components on the same chip. Therefore, various researches have been conducted to find the optimized CMOS-SPAD structure, especially to achieve high sensitivity at near-infrared region (NIR) where ranging technologies are interested. In order to realize the optimized CMOS-SPAD for ranging technologies, accurate device simulation is essential. In this paper, we present two different structures of CMOS-SPAD: based on a shallow junction and deep junction. By using Synopsys Sentaurus technology computer-aided design (TCAD), two CMOS-SPADs are analyzed in terms of E-field profiles and I-V characteristics. Moreover, the breakdown probabilities of the CMOS-SPADs are also investigated to optimize the device structure further.

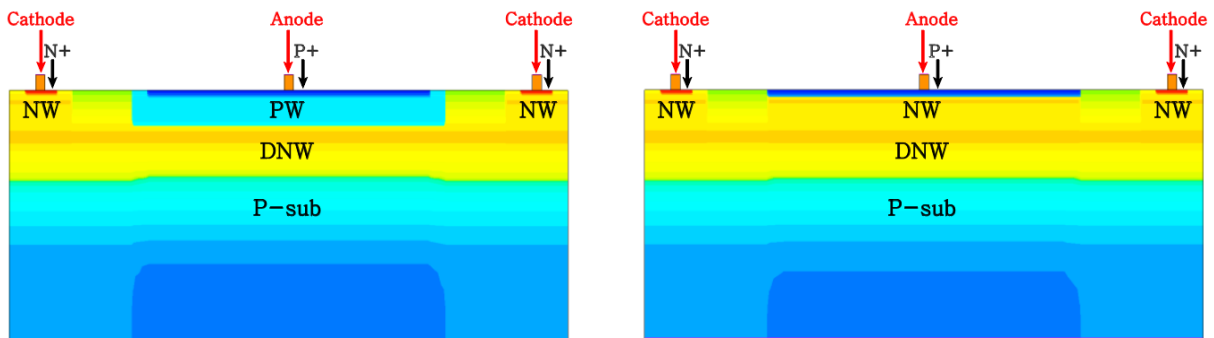


Fig 1. Cross-sections of CMOS-SPADs: (a) with shallow active junction and (b) with deep active junction

## References

[1] Myung-Jae Lee and Edoardo Charbon, "Progress in single-photon avalanche diode image sensors in standard CMOS: From two-dimensional monolithic to three-dimensional-stacked technology," *Japanese Journal of Applied Physics*, (2018).