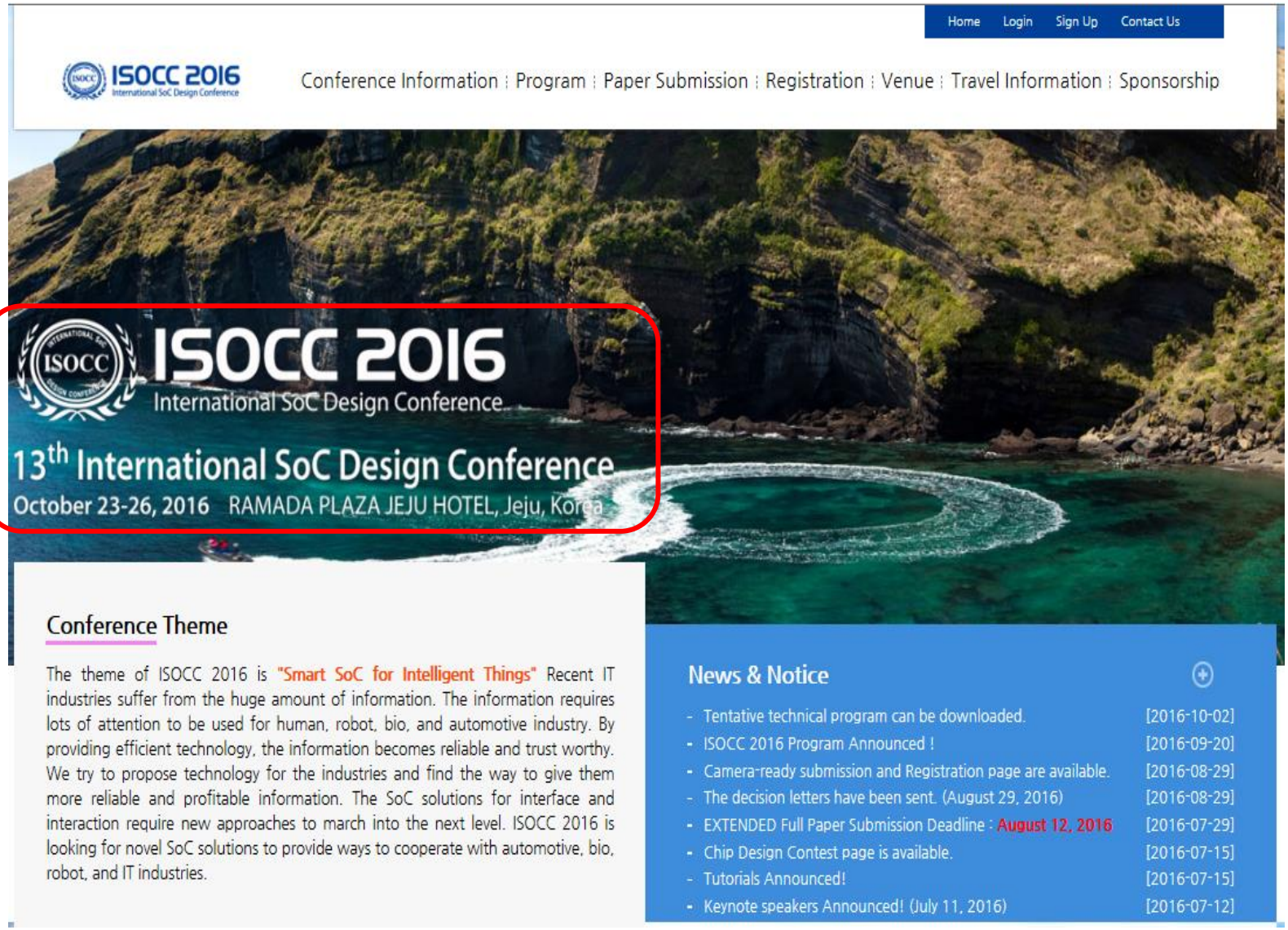
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ISOCC 2016
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International SoC Design Conference
13th International SoC Design Conference
October 23-26, 2016 RAMADA PLAZA JEJU HOTEL, Jeju, Korea
Conference Theme
The theme of ISOCC 2016 is "Smart SoC for Intelligent Things" Recent IT industries suffer from the huge amount of information. The information requires lots of attention to be used for human, robot, bio, and automotive industry. By providing efficient technology, the information becomes reliable and trust worthy. We try to propose technology for the industries and find the way to give them more reliable and profitable information. The SoC solutions for interface and interaction require new approaches to march into the next level. ISOCC 2016 is looking for novel SoC solutions to provide ways to cooperate with automotive, bio, robot, and IT industries.
News & Notice
- Tentative technical program can be downloaded. [2016-10-02]
- ISOCC 2016 Program Announced ! [2016-09-20]
- Camera-ready submission and Registration page are available. [2016-08-29]
- The decision letters have been sent. (August 29, 2016) [2016-08-29]
- EXTENDED Full Paper Submission Deadline : August 12, 2016 [2016-07-29]
- Chip Design Contest page is available. [2016-07-15]
- Tutorials Announced! [2016-07-15]
- Keynote speakers Announced! (July 11, 2016) [2016-07-12]

Sunday ~ Wednesday, October 23~26, 2016

Time		Oct. 23 Sunday		
		2nd Floor		
From	Till	Lobby	Ballroom2	Ballroom3
12:30	13:00	REGISTRATION		
13:00	14:30		Tutorial 1-1	Tutorial 2-1
14:30	14:45		Break	
14:45	16:15		Tutorial 1-2	Tutorial 2-2
16:15	16:30		Break	
16:30	18:00		Tutorial 1-3	Tutorial 2-3
18:00	18:30	Break		
18:30	20:30	Welcom Reception		

Time		Oct. 24 Monday														
			2nd Floor													8th Floor
From	Till		Lobby	Ballroom1	Ballroom2		Ballroom3		Chuja		Mara		Udo			Tamra
8:00	8:15	REGISTRATION	CDC Demo & Panel 1						CDC 1		CDC 2		CDC 3			
8:15	8:30															
8:30	8:45															
8:45	9:00			Break							Break					
9:00	9:15			Opening Ceremony												
9:15	10:00			Keynote 1-1												
10:00	10:45			Keynote 1-2												
10:45	11:00			Break												
11:00	11:45			Keynote 1-3												
11:45	12:30			Keynote 1-4												
12:30	13:45		Lunch													
			Lobby	Ballroom1	Ballroom2		Ballroom3		Ballroom4		Mara		Udo			Tamra
13:45	14:00		CDC Demo & Panel 2		PEC	213	CASE1	173	SS1	052	SS2	050	SS3	195		Intelligent IC Workshop (13:00 ~ 17:30)
14:00	14:15					169		228		019		116		208		
14:15	14:30							029		053		122		222		
14:30	14:45					110		030		059		133		289		
14:45	15:00					124		032				210		288		
15:00	15:15											257				
15:15	15:30			Chip Design Contest (CDC) Poster Exhibition												
15:30	15:45															
15:45	16:00															
16:00	16:15				ARM1	007	DIGITAL1	260	DIGITAL2	127	SS2	258	SS4	201		
16:15	16:30					033		094		074		259		207		
16:30	16:45					152		182				274		236		
16:45	17:00					193		041		129		280		253		
17:00	17:15					232		246		150		281		282		
17:15	17:30					291				027				283		
17:30	18:30															
18:30	19:00		Banquet													
19:00	19:30															
19:30	20:30															

[CDC-P103] An 11-bit 50-MS/s Pipeline ADC Using Circuit-Sharing Techniques

Seungheun Song, Chulkyu Park, Hyunki Jeong, Sanghyung Kim, and Joongho **Choi**
University of Seoul, Korea

[CDC-P104] SIMD Based Multi-Core System-on-Chip Design for Real-Time Signal Processing

Junsang Seo, Inkyu Jeoung, Jaeyoung Kim and Jong-Myon Kim
University of Ulsan, Korea

[CDC-P105] Offset-Canceling Current-Sampling Sense Amplifier for Resistive Nonvolatile Memory in 65-nm CMOS

Taehui Na, Byungkyu Song, and Seong-Ook Jung
Yonsei University, Korea

[CDC-P106] An Implementation of MIMO PHY Modulator for IEEE 802.11n WLAN System

Minjoon Kim, and Jaeseok Kim
Yonsei University, Korea

[CDC-P107] Multi-Rate Clock and Data Recovery Circuit For Display Interface

Ki-Hyun Pyun, Dae-Hyun Kwon, and Woo-Young Choi
Yonsei University, Korea

[CDC-P108] A Single Inductor Multiple Output(SIMO) Buck/Boost DC-DC Converter with Output Error-Driven Random Control

Hyunbin Park, Minseob Sim and Shiho Kim
Yonsei University, Korea

[CDC-P109] Comparison Between Silicon Data and Simulated Data at Near-threshold Region in 65-nm CMOS

Juhyun Park, Hanwool Jeong, Hyun Jun Kim, and Seong-Ook Jeong
Yonsei University, Korea

[CDC-P110] Design of Ka-band Low-noise Amplifier

Mingyo Park, Gyoungjune Jeon and Byung-Wook Min
Yonsei University, Korea

[CDC-P111] Design of Ka-band Power Amplifier

Mingyo Park, Bosung Suh and Byung-Wook Min
Yonsei University, Korea

Multi-Rate Clock and Data Recovery Circuits For Display Interfaces

Ki-Hyun Pyun, Dae-Hyun Kwon, and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea

I. INTRODUCTION

In display applications, the amount of video data rapidly increases due to demands for higher resolution and frame rates, and clock and data recovery (CDR) circuits that can cover multiple data rates are very desirable. Conventional multi-rate CDR circuits consist of the multiple VCOs [1],[2]. However, it is very challenging to design VCOs having the same VCO gain. To solve this problem, a multi-mode phase detector (PD) can be used for multi-rate CDR. We propose a new multi-rate CDR architecture based on a multi-mode rotational bang-bang phase detector (MRBPD), which can operate at 3.5-Gb/s, 7.0-Gb/s and 14-Gb/s.

II. DESCRIPTION

Fig. 1 shows structure of our multi-rate CDR circuit having MRBPD, charge pump, 8-phase VCO, and controller. The controller generates 4-bit signal (T0, T1, T2, T3) depending on FBD0 and FBD1, which represent the data rate. The MRBPD supports full-rate, half-rate and quarter-rate phase detection enabling the multi-mode CDR operation.

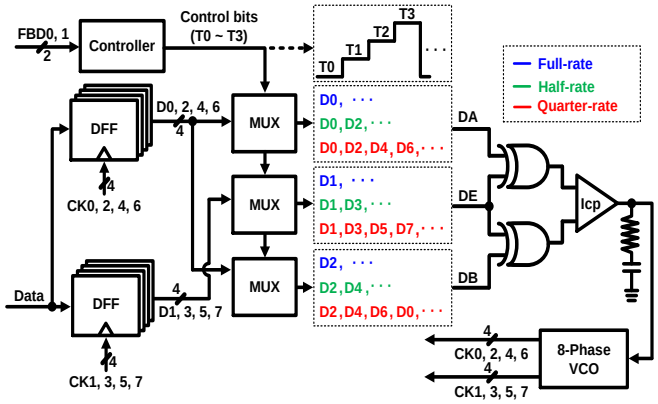

Fig. 1. Proposed multi-rate CDR circuit.

Fig. 2 shows timing diagram for three different data rates. If the data rate is 3.5-Gb/s, the MRBPD operates as a full-rate binary PD. In this case, controller operates in state 1. If the data rate is 7.0-Gb/s, the MRBPD operates as a half-rate binary PD. In this case, controller repeatedly operates in state 1 and state 3 back and forth. If the data rate is 14.0-Gb/s, the MRBPD operates as a quarter-rate binary PD. In this case, controller repeatedly operates in state 1, state 2, state 3 and state 4 rotationally.

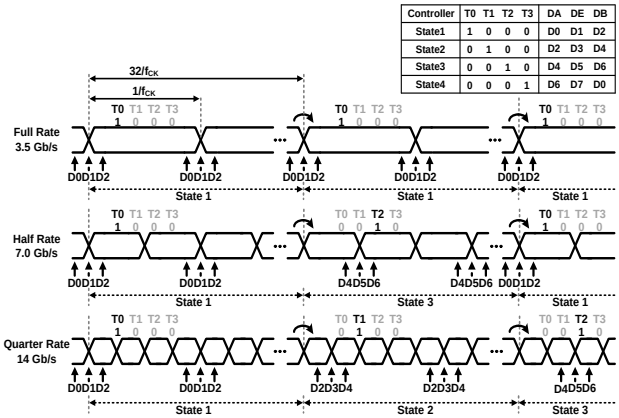

Fig. 2. Timing diagram of multi-rate operation

III. CHIP IMPLEMENTAION AND RESULTS

A die photograph of the CDR is shown in Fig. 2. It is fabricated in 65nm Samsung CMOS process. The CDR occupies 0.017mm^2. Fig. 3 shows measured eye diagram of the recovered output data with full/ half/ quarter-rate operations respectively.

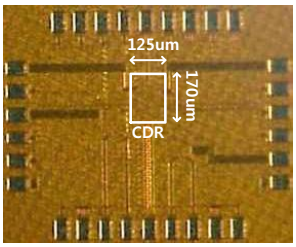

Fig. 3. Photomicrograph of the proposed chip.

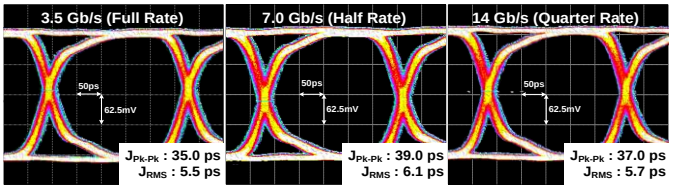

Fig. 4. The eye diagram of recovered data.

REFERENCE

[1] J. Zhou, et al., "A Dual-Mode VCO based Low-Power Synthesizer with Optimized Automatic Frequency Calibration for Software-Defined Radio," in IEEE ISCAS. Papers, May. 2011, pp. 1145-1148..

[2] Y. Dong, et al., "A self-calibrating multi-VCO PLL scheme with leakage and capacitive modulation mitigations," in IEEE ISCAS. Papers, May. 2013, pp. 1400-1403.

This work was supported by the National Research Foundation of Korea grant funded by the Korea government (MEST) [2015R1A2A2A01007772]. The authors are also thankful to IDEC for MPW and EDA software support. Details of our multi-mode CDR will be presented APCAS 2016.

International SoC Design Conference 2016

Multi-Rate Clock and Data Recovery Circuit For Display Interface

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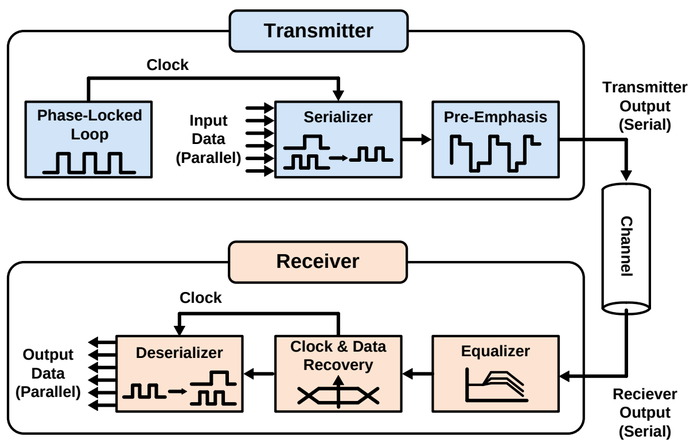
Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

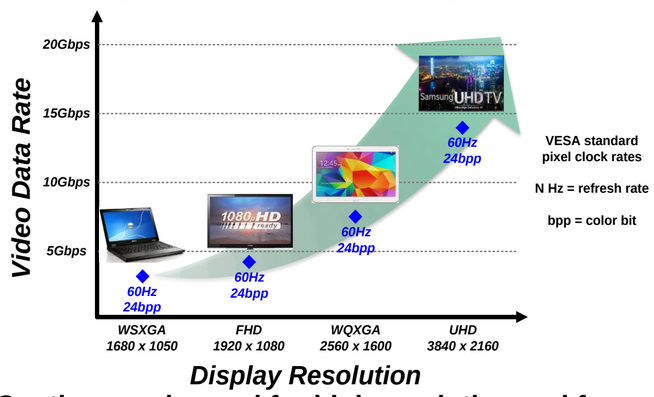
Receiver for Display Interface Applications

High-Speed Serial Link Display Interface

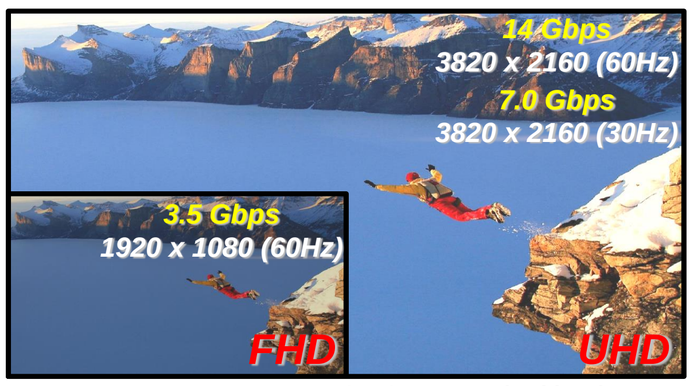
[Block Diagram of Serial Link]



[Display Interface Trends]



- Continuous demand for high resolution and frame rate
  ➔ Support the maximum data rate over 10Gb/s

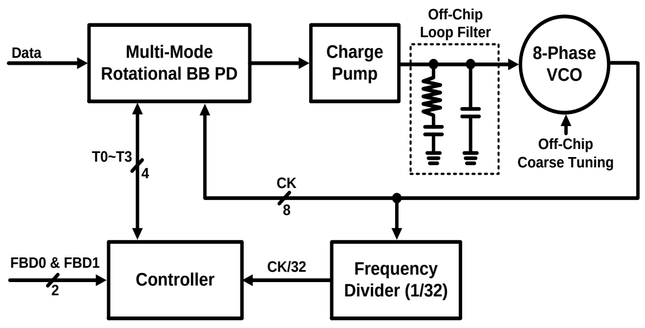


< 16 : 10 aspect ratio video data rate >

- Support FHD 60Hz and UHD 30/60Hz
  ➔ Need multi-rate CDR

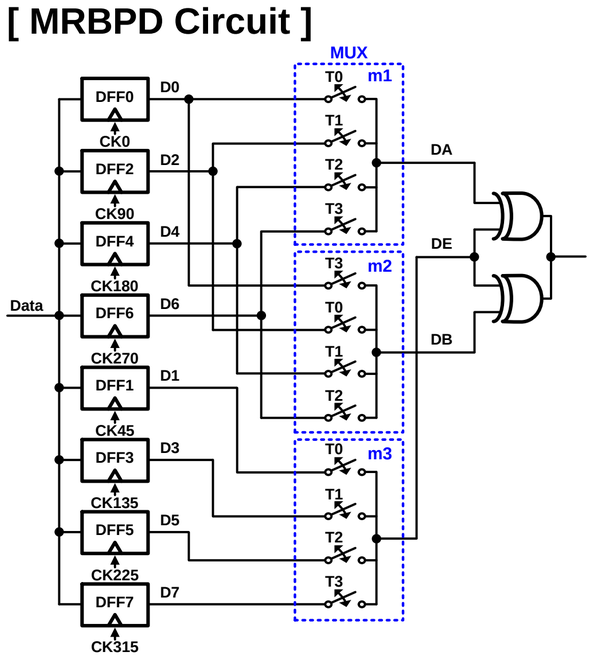
Multi-Rate CDR Design

[Multi-Rate CDR Circuit]



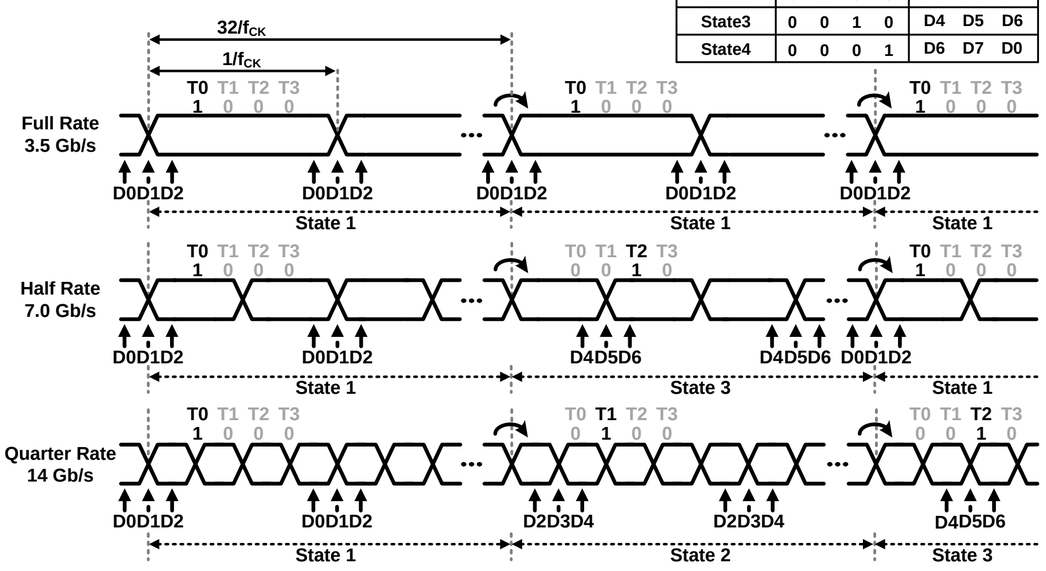
- Multi-Mode Rotational Bang-Bang PD (MRBPD)
- Controller
- Frequency Divider
- 8-Phase VCO
- Charge Pump

[MRBPD Circuit]



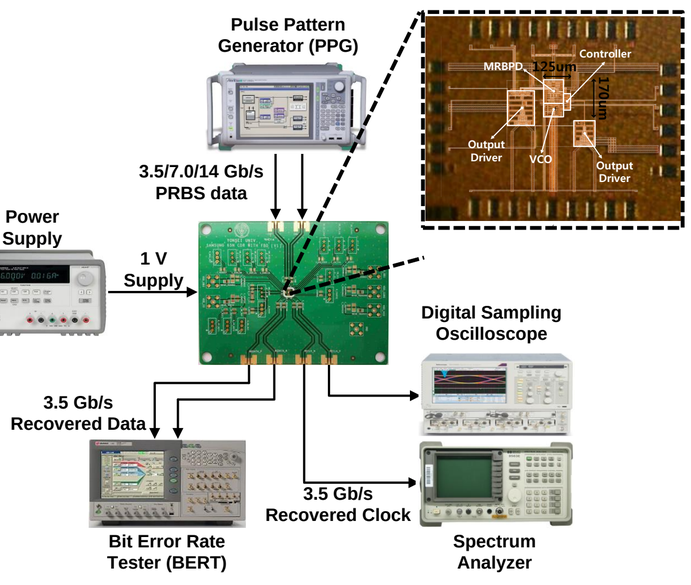
[Timing Diagram]

Controller	T0	T1	T2	T3	DA	DE	DB
State1	1	0	0	0	D0	D1	D2
State2	0	1	0	0	D2	D3	D4
State3	0	0	1	0	D4	D5	D6
State4	0	0	0	1	D6	D7	D0



Measurement Results

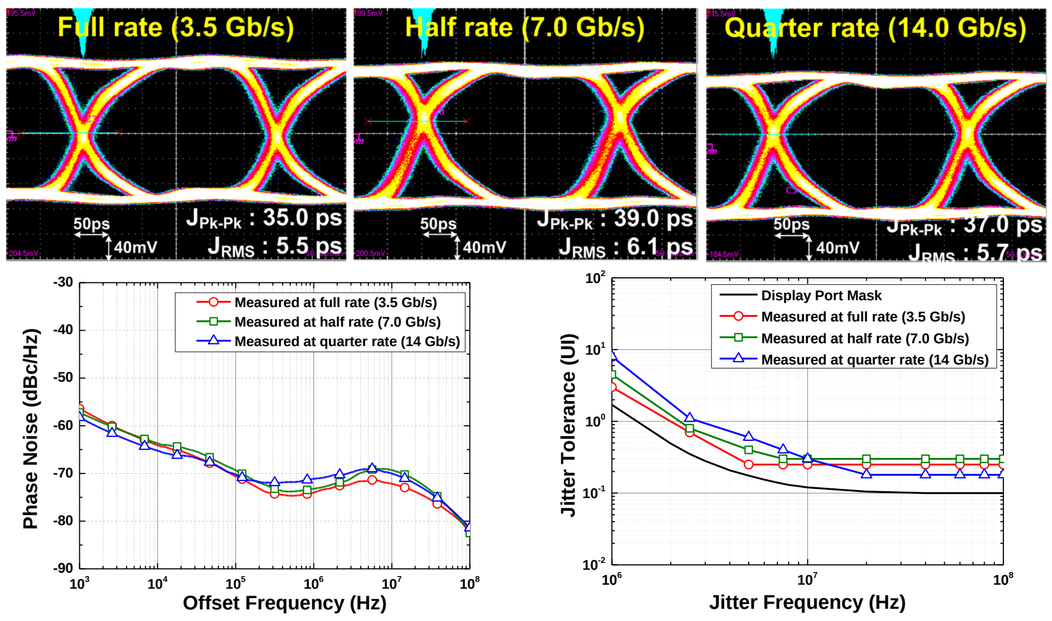
[Experimental Setup]



[Summary]

Data-rate	3.5 / 7.0 / 14.0 Gb/s
Technology	CMOS 65-nm process
Supply Voltage	1.0 V
Core Area	0.025 mm^2
Power consumption	9mW @ 14.0 Gb/s
RMS Jitter	5.7 ps @ 14.0 Gb/s
Power Efficiency	0.64 pJ/bit

[EYE Diagram & Phase Noise & Jitter Tolerance]



Conclusion

- ❖ Multi-rate CDR with multi-mode rotational BBPD is realized in 65-nm CMOS Technology.
- ❖ A multi-mode rotational BBPD can support full-, half-, and quarter-rate phase detection.
- ❖ 3.5-/ 7.0-/14.0-Gb/s data are successfully received with error-free condition.