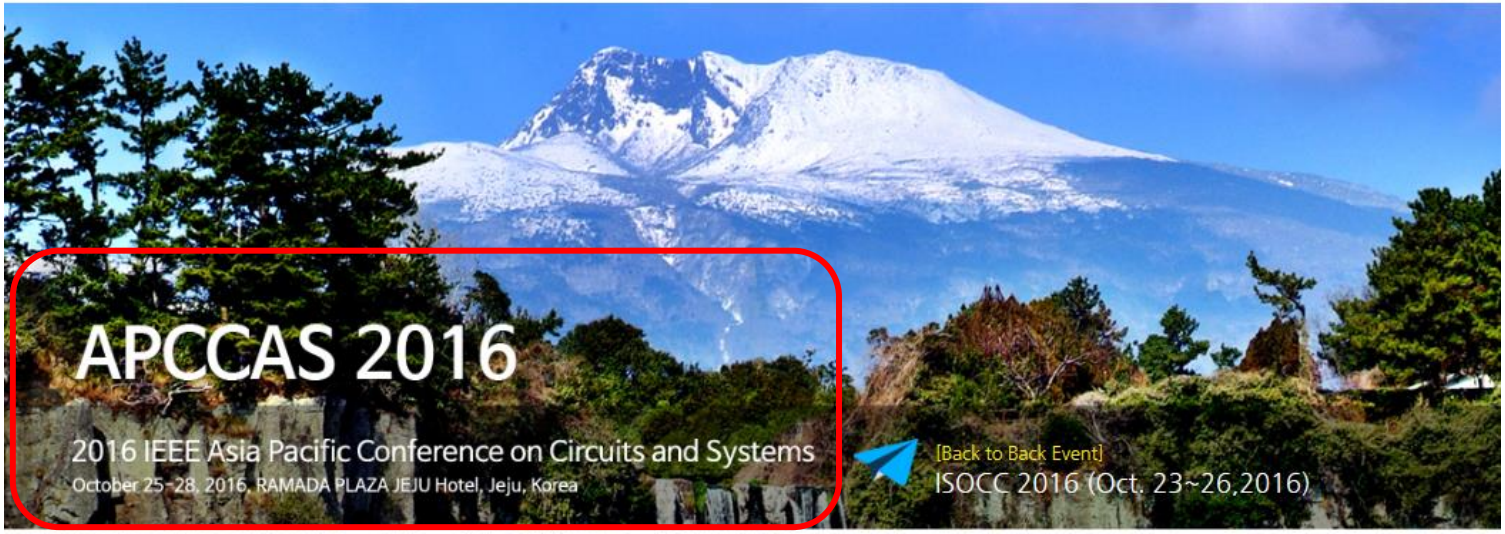
HOME LOGIN SIGN UP CONTACT US

APCCAS 2016

Committee | Paper Submission | Registration | Keynote & Tutorial | Program | For Authors | Accommodation | Jeju | Contact



CONFERENCE THEME

Bringing Tomorrow's Technologies Today: CAS (Creative, Autonomous and Smart) Things

Call For Papers

Aim & Scope

The IEEE APCCAS 2016, the 13th of the biennial Asia Pacific Conference on Circuits and Systems, will be held in Korea at the RAMADA PLAZA JEJU Hotel, Jeju Island. Jeju Island is the biggest island and a most popular tourist resort in Korea. With its natural beauty and unique island culture, Jeju offers cutting-edge convention facilities, sufficient infrastructure, and gifted eco-friendly environment. The APCCAS is a major international forum established by the IEEE Circuits and Systems Society for researchers to exchange their latest findings in circuits and systems.

News & Notice

- "Program at a glance" and Detailed "Session Program" are now available (August 4, 2016).
- Tutorials Announced (July 11, 2016).
- Registration page is available. (July 11, 2016)
- Paper-Submission Deadline Extended to May 15, 2016.
- APCCAS 2016 will offer travel grants for selected students to attend the conference.
- APCCAS 2016: On-line Paper Submission is now OPEN ! (Due date is Apr. 29th)
- Keynote Speakers Announced !
- The selected outstanding papers will be published in IEEE TCAS-I and the River Publishers Book Series

Program at a Glance

Thursday, October 27, 2016

Time		Oct. 27 Thursday						
From	Till	Mara	Udo	Ballroom3	Ballroom4	Lobby	Ballroom2	Others
8:00	18:00	Registration at Lobby						
9:00	10:00	Keynote Speech (Prof. Nikil Dutt)						
10:00	10:20	Coffee Break						
10:20	12:00	B1L-A Multimedia Systems and Applications	B1L-B VLSI Systems & Applications	B1L-C Analysis and Design of Nonlinear Circuits and Systems 1	B1L-D Analog Circuits 2			
12:00	13:30	Lunch Break						Internationmal Steering Committee Meeting of APCCAS and PrimeAsia (12:00-3:00PM) at Biyang
13:30	15:10	B2L-A RF/mm-Wave IC Design and Technology	B2L-B Advanced Signal Processing Circuits and Systems for Communication and Memory Systems	B2L-C Analysis and Design of Nonlinear Circuits and Systems 2	B2L-D Circuits & Systems for Communication 2			
15:10	16:10	Coffee Break				B2P-E Poster Session 2	B2P-F Live-Demo 2 (14:00 - 16:00)	
16:10	17:50	B3L-A Mixed-Signal Circuits 1	B3L-B System-on-Chip and CAD 1	B3L-C Nonlinear Circuits and Systems	B3L-D Circuits & Systems for Communication 3			
18:30	19:30	Banquet at Ballroom						
19:30	20:30							

B2L-D Lecture Session (B2L-D): Circuits and Systems for Communications 2

Date/Time:	**Thursday, 27 Oct 2016/ 13:30–15:10**
Sessions:	**Ballroom4**

Chairs: Chung-An Shen (National Taiwan University of Science and Technology, Taiwan) and
Yin-Tsung Hwang (National Chung Hsing University, Taiwan)

B2L-D-01 Equidistant Mixer-Based Frequency Generation for 60 GHz Fbmc Transmitter Topologies
Oner Hanay, Erkan Bayram, David Bierbuesse, and Renato Negra (Rheinisch-Westfälische Technische Hochschule Aachen, Germany)

B2L-D-02 Design of a 8-Taps, 10Gbps Transmitter for Automotive Micro-Controllers
Andrea Bandiziol (Università degli Studi di Udine, Italy), Werner Grollitsch, Francesco Brandonisio, Roberto Nonis (Infineon Technologies, Austria), and Pierpaolo Palestri (Università degli Studi di Udine, Italy)

B2L-D-03 Digital Clock Data Recovery Circuit for S/PDIF
Jonghoon Kang, and Chanho Lee (Soongsil University, Korea)

B2L-D-04 A 3.5/7.0/14-Gb/s Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Binary Phase Detector
Ki-Hyun Pyun, Dae-Hyun Kwon, and Woo-Young Choi (Yonsei University, Korea)

B2L-D-05 A Multi-Tap Inductor Based 2.0-4.1 GHz Wideband LC-Oscillator
Zaira Zahir, and Gaurab Banerjee (Indian Institute of Science, India)

A 3.5/7.0/14-Gb/s Multi-Rate Clock and Data Recovery Circuit With a Multi-Mode Rotational Binary Phase Detector

Ki-Hyun Pyun, Dae-Hyun Kwon, and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University
Seoul 120-749, Korea
wchoi@yonsei.ac.kr

***Abstract*— A new type of multi-rate clock and data recovery (CDR) circuit is realized that can operate at multiple data rates of 3.5, 7.0 and 14-Gb/s. A multi-mode rotational binary phase detector supports full-rate, half-rate and quarter-rate CDR operation with only one voltage-controlled oscillator. A prototype CDR circuit implemented in 65nm CMOS technology successfully demonstrates the multi-rate operation with energy efficiency of 0.64pJ/bit and chip size of 0.017mm^2, both of which are much less than those of conventional multi-rate CDR circuits.**

Keywords—Binary phase detector, clock and data recovery (CDR), multi-rate operation.

I. INTRODUCTION

The amount of data required for display interface applications is rapidly increasing due to continuous demands for higher resolutions and frame rates. Fig. 1 shows the required video data rates for UHD and FHD resolutions of at several different VESA standard frame rates [1]. As can be seen in the figure, the data rates of 3.5-, 7.0-, and 14-Gb/s are of particular interest for display high-speed serial interface applications.

For these applications, clock and data recovery (CDR) circuits that can operate at multiple data rates are of great interest. Fig. 2 shows the structure of conventional multi-rate CDR circuit having multiple voltage-controlled oscillators (VCOs) [2-4]. With such a structure, it is desired for all the VCOs to have the same gain so that stable CDR dynamics can be achieved. However, designing VCOs operating at different frequencies with the same gain can be very challenging. In addition, power consumption and chip area due to multiple VCOs can be significant. A CDR circuit with a multi-mode phase detector (PD) can solve this problem [5]. However, the PD structure used in [5] is very complex resulting in large power consumption and chip area. It does not allow the full-rate operation either.

We propose a new type of multi-mode PD that is much simpler and supports full, half and quarter-rate operations, resulting much reduced power consumption and chip area. We demonstrate a multi-rate CDR circuit with this multi-mode PD operating at 3.5-, 7.0-, and 14-Gb/s.

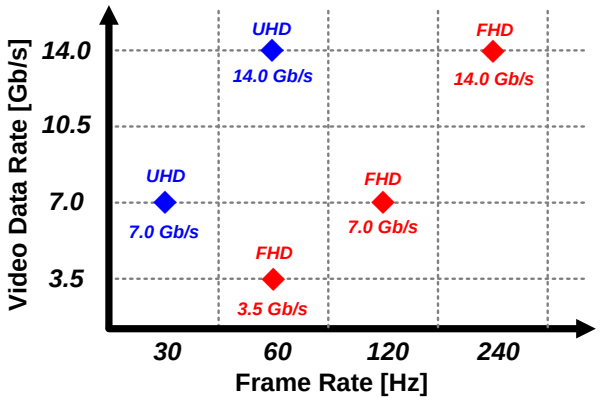


Fig. 1. Video data rate of resolution and frame rate.

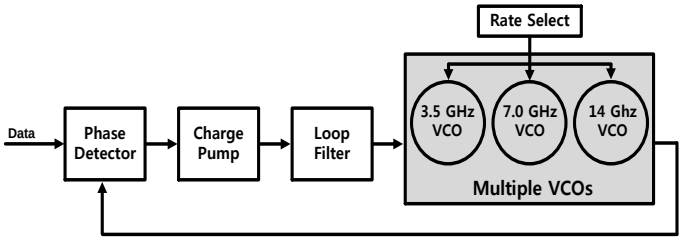
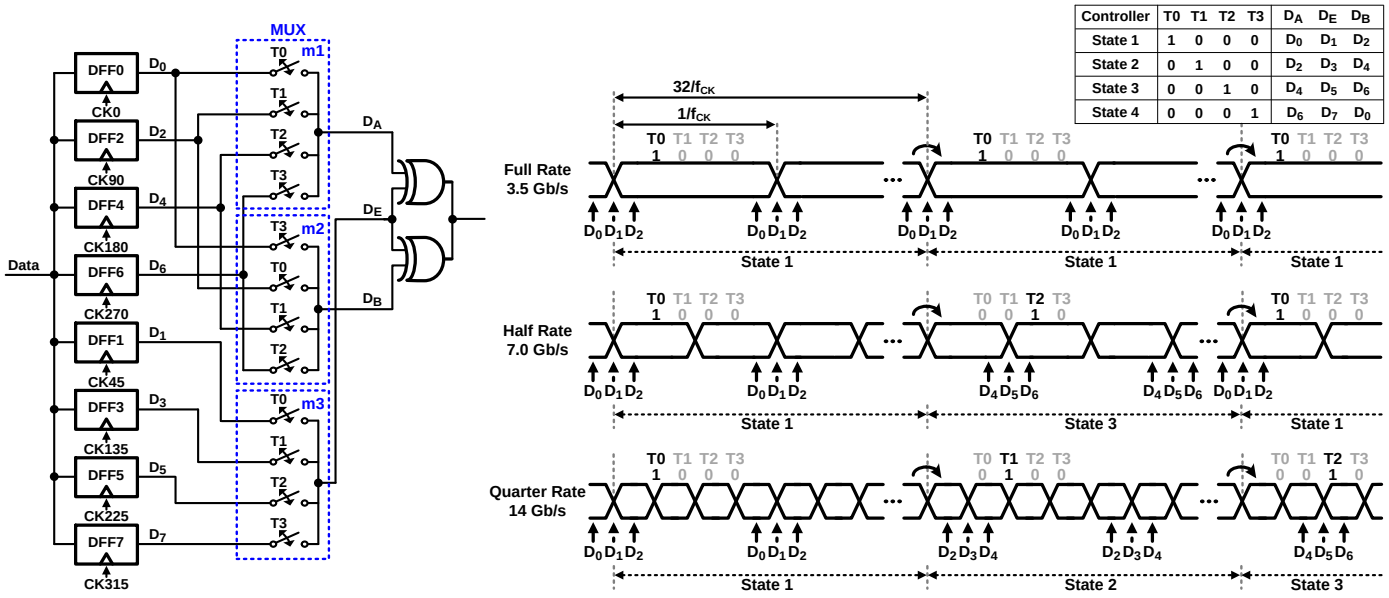


Fig. 2. Conventional multi-rate CDR circuit.

II. CIRCUIT DESIGN

A. Overrall Architecture

The structure of our multi-rate CDR is shown in Fig. 3. It has newly proposed multi-mode rotational binary phase detector (MRBPD), charge pump, 8-phase VCO, frequency divider, and controller. An off-chip loop filter is adopted in our design. The VCO can be tuned from 1.5 to 4.5 GHz with an external coarse tuning voltage. The controller generates 4-bit control signals (T0, T1, T2, T3) which set the operating mode of MRBPD determined by externally supplied FBD0 and FBD1.



(a) (b)

Fig. 4. (a) Multi-mode rotational binary phase detector (b) Timing diagram of the full-rate, half-rate and quarter-rate operation.

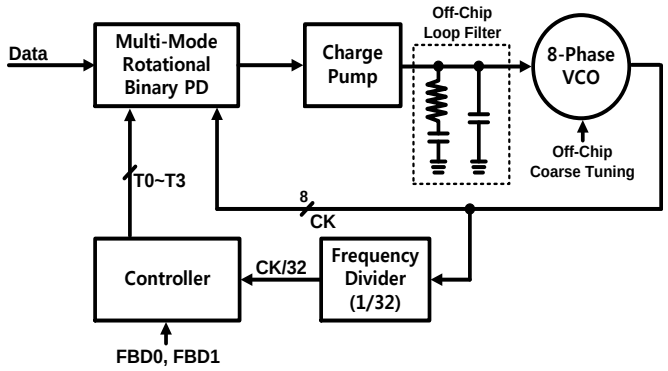


Fig. 3. Proposed multi-rate CDR circuit.

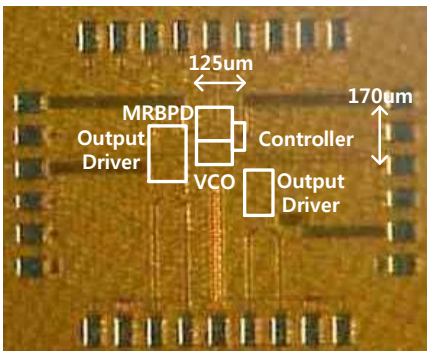


Fig. 5. Die photograph.

B. *Multi-mode rotational binary phase detector*

Fig. 4(a) shows the schematic of our MRBPD. It supports full-rate, half-rate, and quarter-rate phase detection by rotating the 4-bit control signal so that three MUXes (m1, m2, m3) within MRBPD realized with transmission gates produce different output signals depending on the mode. Fig. 4(b) shows timing diagrams for three different data rates. If the data rate is 3.5-Gb/s, the MRBPD operates as a full-rate binary PD. In this case, the controller operates in State 1 and m1, m2, m3 produces D_0, D_1, D_2, respectively. These data are used as inputs of XOR gates, which generate UP and DN pulses. The charge pump uses these pulses to compensate the phase error between received data and recovered clock. If the data rate is 7.0-Gb/s, the MRBPD operates as a half-rate binary PD. In this case, the controller alternates between State 1 and State 3 and m1, m2, m3 produces D_0, D_1, D_2 when in State 1 and D_4, D_5, D_6 when in State 3. If the data rate is 14.0-Gb/s, the MRBPD operates as a quarter-rate binary PD. In this case, the controller rotates among State 1, State 2, State 3 and State 4. Then, m1, m2, m3 outputs are: D_0, D_1, D_2 when in State 1; D_2, D_3, D_4 when in State 2; D_4, D_5, D_6 when in State 3; D_6, D_7, D_8 when in State 4. Since the control signal changes every 32 clock cycles, the data transition detection density of the multi-rate CDR is 1/4 of that of the conventional quarter-rate CDR [8]. However, this should not have a significant influence on CDR performance because rotation of sampling data is much faster than the CDR loop bandwidth. With our MRBPD, several D flip-flops, XOR gates, and charge pumps can be eliminated compared to conventional PD circuits [6-8], resulting in reducing of power consumption and chip area.

III. MEASUREMENT RESULTS

Fig. 5 shows the die photograph of our CDR realized in Samsung 65nm CMOS technology. It occupies 0.017mm^2 except for the output buffer.

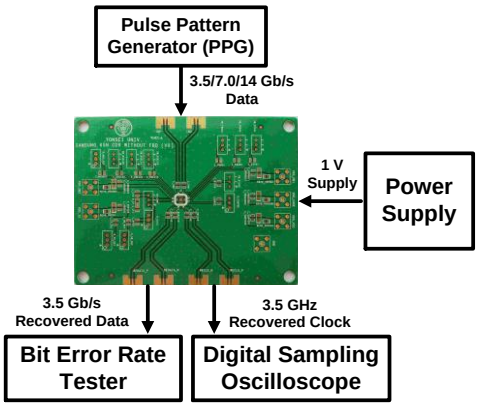


Fig. 6. Measurement set up.

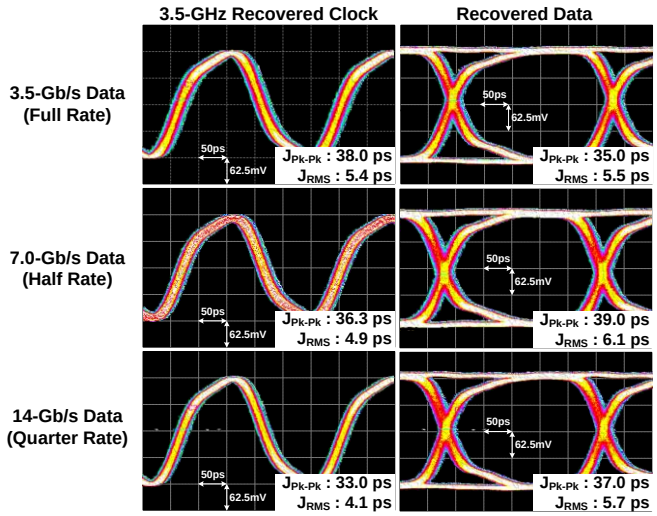


Fig. 7. Measured recovered data and clocks with respect to full-rate, half-rate and quarter-rate operation.

The measurement set up for evaluating CDR performance is shown in Fig. 6. A pulse pattern generator (PPG) produces 3.5-/7.0-/14-Gb/s PRBS 2^{31}-1 data, and recovered clock and data are measured by a digital sampling oscilloscope. The bit error rate tester checks if the CDR produces any errors.

Fig. 7 shows measured eye diagrams for the recovered data and clock for full, half, and quarter-rate operations with 3.5-, 7.0-, and 14-Gb/s input data. Since recovered output data are de-multiplexed by the MRBPD, output data shown in Fig. 7 are all 3.5-Gb/s regardless of the input data rate. The recovered clocks for full/half/quarter-rate operations have peak-to-peak jitter of 38.0/36.3/33.0 ps and RMS jitter of 5.4/4.9/4.1 ps, respectively. The BER is less than 10^{-12} for all three types of operation.

Table I shows performance comparison with a previously reported multi-rate CDR and continuous range CDRs. This is the first CDR with a PD that can operate at three different data rates. Because of this, our CDR is smaller and consumes less power.

TABLE I. PERFORMANCE COMPARISON

	This Work	**2012 [5]**	**2009 [6]**	**2011 [7]**
Data rate [Gb/s]	3.5/7.0/14.0	2.7/5.4	0.65–8.0	0.5–2.5
Process [nm]	65	130	65	130
T_{bit}/T_{clock}	Full/Half/ Quarter Rate	Half/Quarter Rate	Full Rate	Half Rate
Supply [V]	1.0	1.2	N.A	0.8/1.2
Power [mW]	9.0 @ 14.0 Gb/s	104.4 @ 5.4 Gb/s	88.6 @ 8.0 Gb/s	6.1 @ 2.0Gb/s
BER	$< 10^{-12}$	$< 10^{-12}$	$< 10^{-12}$	$< 10^{-12}$
Recovered Clock RMS Jitter [ps]	5.4 @ 3.5 Gb/s 4.9 @ 7.0 Gb/s 4.1 @ 14.0 Gb/s	4.0 @ 2.7 Gb/s 3.2 @ 5.4 Gb/s	9.7 @ 8.0 Gb/s	5.4 @ 2.0 Gb/s
Power Efficiency [pJ/bit]	0.64	19.30	11.07	3.05

ACKNOWLEDGMENT

This work was supported in by the National Research Foundation of Korea [MEST 2015R1A2A2A01007772] and Samsung Electronics. The authors are also thankful to IDEC for MPW and EDA software support.

REFERENCES

[1] DisplayPort Standard Version 1.2, Jun.2007, Video Electronics Standard Association.

[2] Y. Tsunoda, *et al*., "A 24-to-35Gb/s x4 VCSEL Driver IC with Multi-Rate Referenceless CDR in 0.13μm SiGe BiCMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 414-415.

[3] J. Zhou, *et al*., "A Dual-Mode VCO based Low-Power Synthesizer with Optimized Automatic Frequency Calibration for Software-Defined Radio," in *IEEE ISCAS. Papers*, May. 2011, pp. 1145-1148..

[4] Y. Dong, *et al*., "A self-calibrating multi-VCO PLL scheme with leakage and capacitive modulation mitigations," in *IEEE ISCAS. Papers*, May. 2013, pp. 1400-1403.

[5] W. Y. Lee, *et al*., "A 5.4/2.7/1.62-Gb/s Receiver for DisplayPort Version 1.2 With Multi-Rate Operation Scheme", *IEEE Trans. Circuits and Systems−I: Regular Papers*, vol. 59, no. 12, pp. 2858−2866, Dec. 2012.

[6] S. Lee, *et al*., "A 650Mb/s-to-8Gb/s referenceless CDR circuit with automatic acquisition of data rate," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 184-185.

[7] R. Inti, *et al*., "A 0.5-to-2.5 Gb/s Reference-Less Half-Rate Digital CDR With Unlimited Frequency Acquisition Range and Improved Input Duty-Cycle Error Tolerance," *IEEE J. Solid-Stage Circuits*, vol. 46, no. 12, pp. 3150−3162, Dec 2011.

[8] L. Rodoni, *et al*., "A 5.75 to 44 Gb/s Quarter Rate CDR With Data Rate Selection in 90nm Bulk CMOS," *IEEE J. Solid-Stage Circuits*, vol. 44, no. 7, pp. 1927−1941, July 2009.